Chapter 1 General

1.1 System Overview

The uPD72070 Floppy Disk Controller (FDC) is a new advanced Floppy Disk Controller that can support four standard Floppy Disk Drives (FDD)'s and two Apple specific FDDs, respectively. For the standard FDDs, the uPD72070 FDC is compatible with the NEC µPD765A and therefore maintaining compatibility with all uPD765A existing software and copy protection schemes.

The uPD72070 FDC has the special capability to support both writing and reading the Apple proprietary GCR format. In addition the uPD72070 can support conventional MFM and FM formats in the 2DD, 2HD, 2ED and 2TD typed FDDs. These features make the uPD72070 FDC easily adaptable into Apple Macintosh computers.

By having the same register set as in the IBM PS/2 and PC/AT computers, the uPD72070 FDC can easily be adapted in these PCs and compatible PCs.

The external circuits necessary to support both Apple Computers standard Super Drive FDD's and conventional MFM FDDs are fully implemented into the uPD72070 FDC.

1.2 Features

The 72070 Advanced Floppy Disk Controller or "New Age FDC" has the following features.

- General
  - Functional superset of µPD765A and Intel 82077
  - Supports Apple GCR format
  - Supports 1MB, 2MB, 4MB and 13MB FDDs
  - Automatic wake up from standby mode• Host Interface
  - 8-bit BUS width
  - 16-byte FIFO in the Data register
  - Implements PS/2 and PC/AT registers

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  - 8-bit BUS width
  - 16-byte FIFO in the Data register
  - Implements PS/2 and PC/AT registers

- Intel Interface
- Drive Interface
  - Supports both the Apple specific FDDs and standard FDDs
  - Analog PLL based on μPD72069
  - Precompensator
  - Clock Generator
  - FDD drivers and receivers
- Additional commands
  - Apple specific commands

  (These should be disclosed only to Apple Computer)

1.3 Recording Formats

This FDC can support the following two formats:

1) GCR recording format used on special FDDs in Apple Macintosh Computers
2) MFM and FM recording formats used on conventional FDDs and Super Drives in Apple Macintosh Computers

1.3.1 GCR Format Description (Group Code Recording)

GCR is the older of the two floppy disk formats used in Macintosh computers. Disks formatted with GCR can store up to 800K bytes on a double sided disk. In the GCR encoding scheme, only binary 1's generate transitions (Figure 1.3.1). A long run of zeroes, leading to an absence of transitions, can make the data recovery process very difficult and unreliable. In order to improve the reliability of data recovery, the software driver code (referred to as the driver), encodes the data to limit the maximum number of non-transitions to 2. Apple calls this process nibblizing, and if effectively encodes 3 bits of raw data into 4. When the driver reads data from the disk, it decodes it by a process called denibblizing.

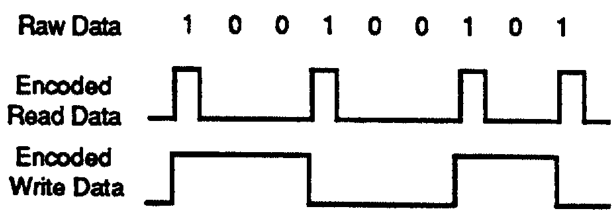


Fig. 1.3.1 GCR Encoded Read and Write Data

1.3.1.1 GCR Track and Sector Format

In order to maximize the storage capacity of a GCR floppy disk, GCR drives vary their spindle speed by making automatic adjustments based on the cylinder. This permits greater storage for the outer cylinders than could be achieved if the spindle speed were held constant. As a simplification, the 80 cylinders on a GCR drive are split up into 5 speed zones, each with a different number of formatted sectors(Table 1.3.1).

Table 1.3.1 GCR Speed Groups

Speed Zone	Cylinders	Sectors
1	0 to 15	12
2	16 to 31	11
3	32 to 47	10
4	48 to 63	9
5	64 to 79	8

The driver formats a disk so that the sectors are evenly distributed around each track(Figure 1.3.2). This is accomplished by varying the number of sync groups between the sectors of the track. A sync group is composed of a 6 byte sequence(FF 3F CF F3 FC FF) which guarantees that the hardware is synchronized prior to the beginning of an address or data mark.

During the format process, the driver initially tries to format the track with 6 or 7 sync groups between sectors. If that is successful, the driver will increment the number of sync groups and reformat the track. If that format is successful, the process is repeated until the format fails. Once the format has failed, the driver uses the last successful number of sync groups to format the track.

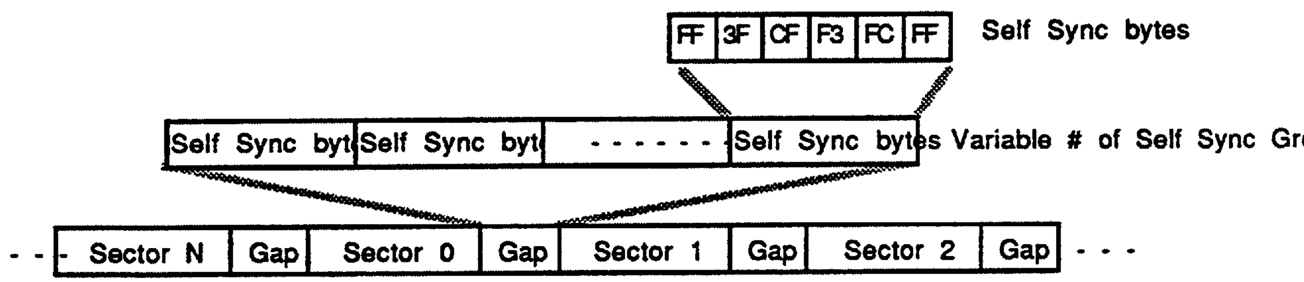


Fig. 1.3.2 GCR Track Format

Figure 1.3.3 shows the GCR sector format. Both parts of the sector begin with six self sync bytes. The address field consists of three mark bytes($D5, $AA, $96); the track, sector, side, format and checksum bytes(encoded as GCR nibbles); and two bit slip bytes ($DE, $AA). The track and side information are combined into a 16-bit word that puts the side number into bit 11 and the track number into bits 0-10. Although 11 bits are specified for the track number, only 8 bits are used. The remaining 3 bits, track 10-8, are always 0.

The data field consists of three mark bytes($D5, $AA, $AD), the sector number, sector data, and two bit slip bytes($DE, $AA). The sector data consists of: 12 tag bytes (used by the operating system), 512 data bytes (containing user data), and 3 checksum bytes. When encoded as GCR nibbles, the data tales up 703 bytes:4*[(12+512)/3 groups]=699 data+4 checksum bytes.

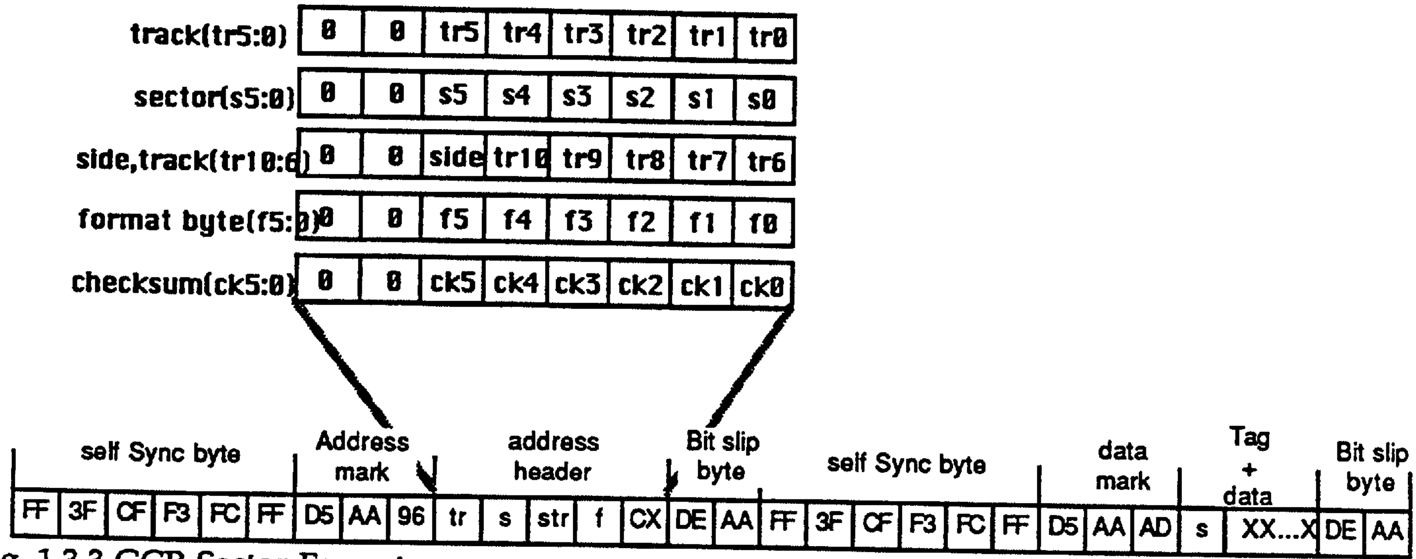


Fig. 1.3.3 GCR Sector Format

1.3.1.2 Nibblizing and Denibblizing

As mentioned in the previous section, data written to the disk must be encoded in order to limit the "0" run length of the serial bit stream. When data is written it is nibblized, and when it is read it is denibblized. Because of the size of the address field, the driver encodes the data and address header differently. The nibblizing and denibblizing processes for each will be discussed separately.

1.3.1.3 Nibblizing Sector Data

GCR sector data contains two parts: Tag Bytes and Sector Data (see the section on GCR sector format for more details). The operating system uses the 12 bytes for various functions. While, the sector data merely contains 512 bytes of user data. Between the two, the total length of the sector data field is 524 bytes. Therefore, the driver must nibblize 524 bytes when it writes the sector data.

The nibblizing process(US patent #4,564,941 Wooley et al, Apple Computer Inc.) begins by reading 3 bytes of data in order to encode them into 4 bytes. The encoding guarantees that the four bytes do not exceed the run length restriction of the GCR encoding specification. As a convention, the bytes in this 3 byte group are referred to as the A byte, B byte, and C byte.

Nibblizing is performed in a two stage process. In the first stage the driver accumulates the checksums for the 3 bytes of data. When computing the

overall checksum for the data, the driver maintains three checksums; the A, B, and C checksum, that correspond to the A, B, and C bytes. The algorithm for this is shown below on pseudocode:

```
/* Reads Data from the System Memory */
For (n=0; n=<0x20b ; n++)       /* repeats 524 times */
    Read( Data(n) );            /* reads data from the System
                                   Memory into Data (n) */
    Data(0x20c)=0;              /* the only last data should be set to
                                  zero */
/* Initialization */
ChecksumA =0 ;
ChecksumB =0 ;
ChecksumC =0 ;
Carry_ChecksumCx =0 ;           /*the Carry bit of ChecksumCx */

For ( n=0; n=< 0x0ae ; n++)     /* repeats to calculate 175 times */

    ByteA=Data(n);
    ByteB=Data(n+1);
    ByteC=Data(n+2);

    ChecksumA=ChecksumA + ByteA + Carry_ChecksumCx;
    ByteA =ByteA XOR ChecksumC;

    ChecksumB=ChecksumB + ByteB + Carry_ChecksumA;
    ByteB =ByteB XOR ChecksumA;

    ChecksumCx=ChecksumC + ByteC + Carry_ChecksumB;
    ByteC =ByteC XOR ChecksumB;

    ChecksumC=Rotate Left 1, not through Carry_ChecksumCx;
```

It is important to notice in the pseudocode above that there is interaction

amongst both the checksums and the data. This is done to improve the error detection capability of the algorithm. In order to properly encode the data, the driver must adhere to this exact sequence of operations. Violating the sequence will cause encoding errors.

In the second stage of the process, the 3 bytes are encoded to limit the "0" run length of the data prior to writing in to disk. Fig. 1.3.4 shows the second stage of the nibblizing process.

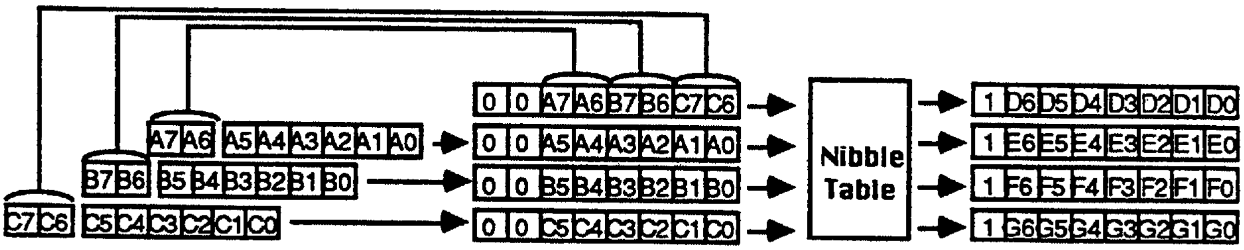


Fig. 1.3.4 Nibblizing process for Sector Data

The driver strips of the two upper bits of each of the three bytes and accumulates them in a fourth byte, called the Hi-Bits byte. The driver then encodes each of these four bytes with the Nibblizing look up table shown in Table 1.3.2. For example, applying the byte $0F(001111 in binary) to the table yields an encoded byte of B3H. After the driver encodes each byte, they are written to the disk serially, with the most significant bit written first. Because the driver computes the checksums prior to the Hi-Bits byte.

Table 1.3.2 Nibblizing Look-Up Table

Bits 2:0

Bits 5:3	000	001	010	011	100	101	110	111
000	$96	$97	$9A	$9B	$9D	$9E	$9F	$A6
001	$A7	$AB	$AC	$AD	$AE	$AF	$B2	$B3
010	$B4	$B5	$B6	$B7	$B9	$BA	$BB	$BC
011	$BD	$BE	$BF	$CB	$CD	$CE	$CF	$D3
100	$D6	$D7	$D9	$DA	$DB	$DC	$DD	$DE
101	$DF	$E5	$E6	$E7	$E9	$EA	$EB	$EC
110	$ED	$EE	$EF	$F2	$F3	$F4	$F5	$F6
111	$F7	$F9	$FA	$FB	$FC	$FD	$FE	$FF

The encoding process described above assumes that data portion of the sector is evenly divisible by 3. Unfortunately this is not the case. Because

the sector data field is 512 bytes long, the driver must handle the residual 2 bytes as a special case. In order to properly encode the last 2 bytes of the sector data, the driver assumes that a 513th byte is zero. Therefore, the driver encodes that last two bytes assuming a third byte which is zero. The driver dose not write this zero byte to the disk.

After the driver wries that last data to the disk, the driver nibblizes the three checksum bytes(as shown in Figure 1.3.4), and writes them to the disk.

1.3.1.4 Denibblizing

When the driver reads data from the disk it must be decoded before it can be used. Apple calls this process denibblizing. The driver denibblizes the read data in two stages.

In the first stage the driver reads four data bytes from the disk. The driver must work in blocks of four bytes because the nibblizing process encoded three byres into four. As the bytes are read from the disk, the driver initially decodes them with the look-up table in Table 1.3.3. For example, a data byte of $B9 is decoded to $14.

Bits 3:0 \ Bits 7:4	$9	$A	$B	$C	$D	$E	$F
$0	-	-	-	-	-	-	-
$1	-	-	-	-	-	-	-
$2	-	-	0E	-	-	-	33
$3	-	-	0F	-	1F	-	34
$4	-	-	10	-	-	-	35
$5	-	-	11	-	-	29	36
$6	00	07	12	-	20	2A	37
$7	01	08	13	-	21	2B	38
$8	-	-	-	-	-	-	-
$9	-	-	14	-	22	2C	39
$A	02	-	15	-	23	2D	3A
$B	03	09	16	1B	24	2E	3B
$C	-	0A	17	-	25	2F	3C
$D	04	0B	18	1C	26	30	3D
$E	05	0C	19	1D	27	31	3E
$F	06	0D	1A	1E	28	32	3F

Table 1.3.3 Denibblizing look-up table

After the decode through the look-up table, the data is now composed of 4 bytes with their two most significant bits to zero. The driver then takes the first of the 4 bytes(the Hi-Bits byte) and re-distributes the data, in two bit chunks, across the remaining three bytes. Figure 1.3.5 shows the complete decoding process.

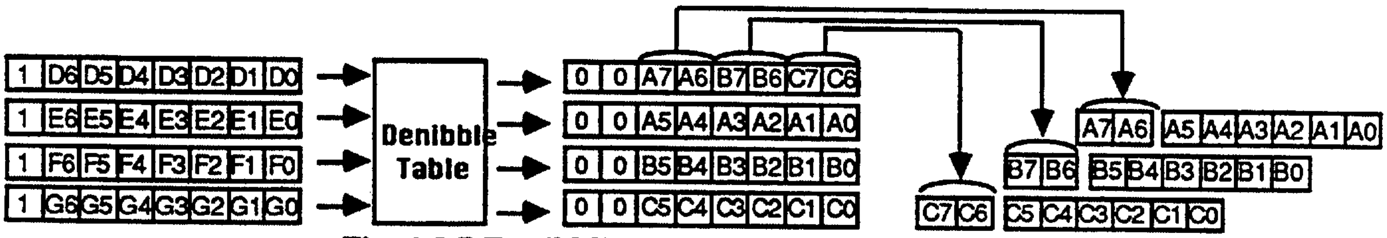


Fig. 1.3.5 Denibblizing process for Sector Data

Now that the original three have been reassembled, the driver must compute and compare the checksums. The pseudocode example below shows the algorithm for computing the checksum during a read.

```
/* Reads Read-Data from the FDD */
For (n=0; n=<0x2bb ; n++)      /* repeats 700 */
    Read( Byte(n) );           /* reads Read-data from the FDD
                                  into Data (n) after denibblization */
/* Initialization */
ChecksumA =0 ;
ChecksumB =0  ;
ChecksumC =0 ;

For ( n=0; n=< 0x0ae ; n++)    /* repeats to calculate 175 times */
    Carry_CheksumC =ChecksumC(bit7);
    ChecksumC=Rotate Left 1, not through carry (ChecksumC);

    Byte(n)=Byte(n) XOR ChecksumC;
    ChecksumA=ChecksumA + Byte(n) + Carry_ChecksumC;

    Byte(n+1)=Byte(n+1) XOR ChecksumA;
    ChecksumA=ChecksumA + Byte(n+1) + Carry_ChecksumA;
```

Byte(n+2)=Byte(n+2) XOR ChecksumB;

ChecksumA=ChecksumA + Byte(n+2) + Carry_ChecksumB;

Data(n) =Byte(n);

Data(n+1)=Byte(n+1);

Data(n+2)=Byte(n+2);

The denibblizing process assumes that the number of bytes the data field are evenly divisible by 4. Unfortunately, because of the assumed 513th data byte (see the previous section, which was not written when the driver encoded the data, there will be a residual of 3 bytes during the read. In order to properly decode the last three bytes, the driver assumes a "0" byte that is not read from the disk. The driver decodes that last three bytes and the assumed "0" byte the same process shown in Figure 1.3.5.

After the driver has read, decoded, and reassembled all the data bytes, the four checksum bytes are denibblized by the same process that is shown in Figure 1.3.5. The driver then compares the computed checksum against the reassembled three checksum bytes.

1.3.1.5 Nibblizing and Denibblizing for the Address Header

Because of the small number of bytes in the address header, the driver encodes the address header differently from the data field. In general, the process for the address header is much less complicated. As shown in Figure 1.3.3, the driver formats the of the address header so that they have their upper two bits set to zero, with the data occupying the lower 6bits of the byte. This format simplifies the nibblizing process by making the Hi-Bits byte process unnecessary. The driver can simply encode the 4 bytes directly through the nibblizing table. In addition the checksum computation is also significantly simplified. To compute the checksum, the driver merely xor's all four bytes into a longitudinal checksum according to the following algorithm:

Checksum : = track byte xor sector byte xor side, track byte xor format byte;

All four bytes and the checksum byte are then encoded with the look-up table in Table 1.3.2 and written to the disk. Figure 1.3.6 shows the nibblizing process for the address header and its checksum.

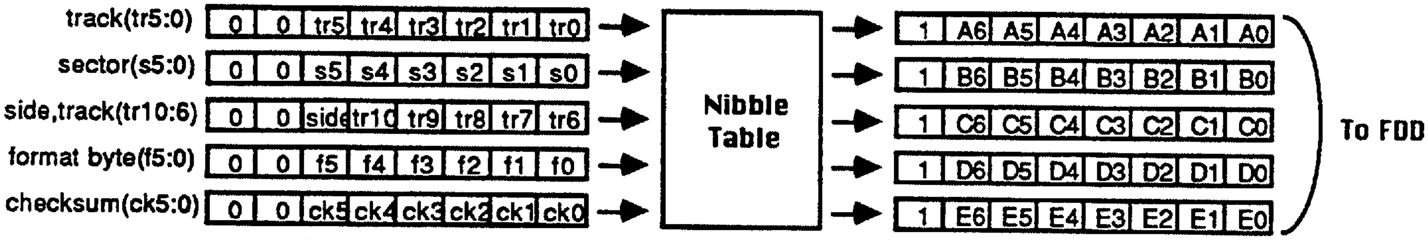


Fig. 1.3.6 Address Header Nibblizing Process

When the driver reads the address header, the driver simply decodes each byte with the denibble table shown in Table 2-3. Figure 2-7 shows the denibblizing process for the Address header.

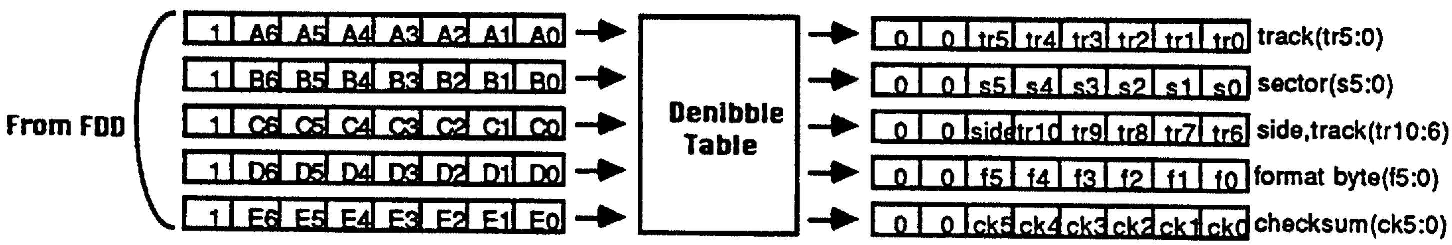


Fig. 1.3.7 Address Header Denibblizing Process

The driver then computes and compares the checksum according algorithm shown above.

1.3.1.6 Error Detection for GCR

The following conditions should be reported as errors:

- Partial Address Mark

  The address mark found is not complete.
- Bad Address Checksum

  The computed checksum does not match the checksum stored at the end of the address header of the sector.
- Bad Address Bitslip Marks

  The bitslip bytes at the end of the address header do not meet the format specification.
- Bad Data Mark

  The data mark of the sector is not complete.

- Bad Data Checksum

  The computed checksum dose not match the checksum stored at the end of the data portion of the sector.
- Bad Data Bitslip Marks

  The bitslip bytes at the end of the data portion of the sector do not meet the format specification.

1.3.2 MFM Description

Unlike GCR drivers, MFM drivers do not vary their spindle speed while writing or reading data on a disk. Instead, the driver puts the same number of sectors on each track. For the 720K format, there are 9 sectors per track and for the 1440K format, there are 18 sectors per track. The disk drive does vary its spindle speed for the different MFM densities; 600 rpm for 720k, or 300 rpm for 1440k.

1.3.2.1 MFM Track and Sector Format

Fig. 1.3.2.1 shows the MFM track format The driver uses the index pulse to determine where the track physically begins. In order to maintain compatibility with the NEC µPD765A disk controller format, the driver writes index information during the time that the index pulse is asserted. The index field is made up of 12 bytes of zeroes which is followed by the index mark. The index mark is composed of three special characters($C2) and the byte pattern $FC. These special characters violate the MFM encoding standard by missing a transition. Once the index information is written is ignored by any subsequent operations.

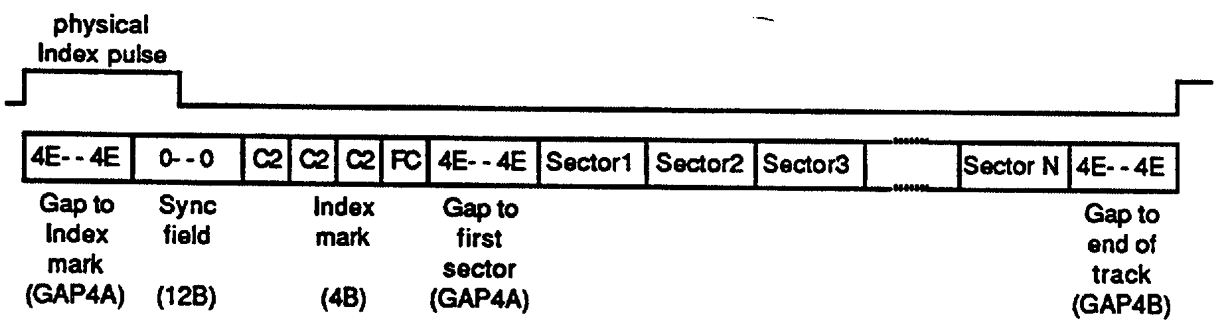


Fig. 1.3.2.1 MFM Track Format

Following the index information, the MFM track format contains a gap that acts as a buffer to allow for drive variations. Depending on density, the driver formats either 9(720K) or 18(1440K) sectors following the gap. Following the last sector, the driver writes gap bytes to the end of the track. Fig. 1.3.2.2 shows the MFM sector format.

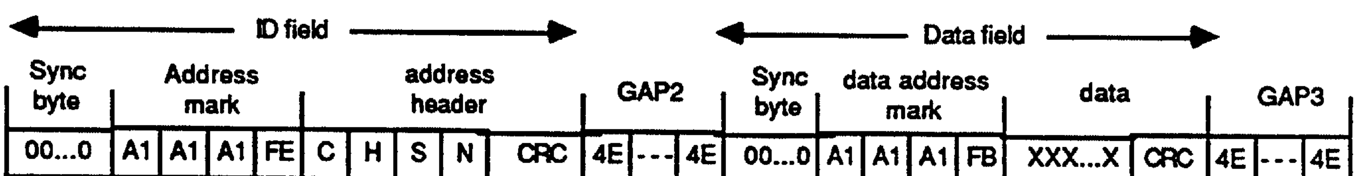


Fig. 1.3.2.2 MFM Sector Format

A track contains 5 distinct gaps that vary depending upon format density. Table 1.3.2.1 shows the gap sizes for all the gaps shown in Figures 1.3.2.1 and 1.3.2.2, organized according to the disk density.

Disk Capacity		Gap length in Bytes				
Unformatted	Formatted	Gap1	Gap2	Gap3	Gap4A	Gap4B
1MB	720KB	50	22	84	80	182
2MB	1.44KB	50	22	101	80	204
4MB	2.88MB	50	41	83	80	518

Table 1.3.2.1 Gap sizes for Various MFM disk capacities

1.3.2.2 CRC Computation for MFM

The CRC computation for both the address header and sector data follow the CCITT-CRC16 algorithm.

1.3.2.3 Precompensation of MFM Data

For industry standards, one precompensation value is used with MFM. The 1Mbyte and 2Mbyte disks(720K and 1.44M formatted disks) require 125ns for inner cylinders. The 4MByte disk standard does not require any precompensation. The precompensation values are defined by the bits in the Data Rate register.

1.4 Operation Modes

This FDC can support the following operation modes by using the external PCTYP1,0 pins:

PCTYP1	PCTYP0	Operation Mode	
1	1	Apple	- Selects Active Low Reset
1	0	General	- Standard Mode
0	0	PS/2	- Standard Mode
0	1	PC/AT	- Standard Mode

In each mode, there are different ways available for Registers and Commands to be used. Therefore, the host should use the following functions according to the operation mode:

- Formats	- Data rates	- Motor On/Off
- Drive Select	- Precompensation	

1.4.1 Apple Mode

This Apple mode implemented into the uPD72070 FDC is available only for Apple Computer and may not be available for other users of this FDC.

Under Apple mode, only the Status register (STR), Data register (DTR) and Data rate register (DRR) can be used.

GCR recording formats are support on the Macintosh FDD's which include the Apple Super Drive and emerging Apple 4MB Super Drive FDD. MFM recording formats are supported on 1MB, 2MB, and 4MB FDD's. (There is no support for FM recording formats)

As for the commands, the FDC can support the all commands except the following commands:

- Read Deleted data	- Write Deleted data	- Scan Equal
- Scan Low or Equal	- Scan High or Equal	- Verify
- Relative Seek	- Dumpreg	- Version

As for the Data Rates, the bits (DRATE1, DRATE0) in the Data Rate Register should be set.

As for the target drive, the bits (DR1, DR0) in the issued commands can automatically select the desired drive so that the polling function can be supported.

As for the formats, the (FM) bit in the issued commands can automatically select either GCR or MFM formats.

As for turning the FDD motor On or Off, the Set Motor Control command should be used.

GCR recording requires no preshifting of the Write Data signal from the FDC.

The Data Register with FIFO will always be available in the Execution phase of the Read/Write commands group after the EFO bit and the FIFOTHD bits in the Configure command are set.

The combination of Select Drive Type and Perpendicular Mode commands, in conjunction with the setting of the proper bits in the Data Rate Register (DRR) register are used to select the types Floppy Disk Drive to be used. Selection can be one of the following drives; 2DD, 2HD, 2ED, 2TD and GCR. Please refer to Table 1.4.1.2.

Also, the reference table of various media for different disk capacity, data rate, & track number is shown on table 1.4.1.1.

Media	Capacity	RPM	Data Rate	Track (Cylinder)	Sector	Byte/Sector
USA (IBM DOS)						
5.25"	1.2M (1.6M)	360	500K	160 (80)	15	512
3.5"	720K (1M)	300	250K	160 (80)	9	512
3.5"	1.44M (2M)	300	500K	160 (80)	18	512
3.5"	2.88M (4M)	300	1M	160 (80)	36	512
JAPAN						
5.25"	640K	360	300K	160 (80)	8	512
5.25"	1.2M	360	500K	154 (77)	8	1024
3.5"	640K	360	300K	160 (80)	8	512
3.5"	1.2M	360	500K	154 (77)	8	1024

Table 1.4.1.1 Capacity, RPM, Data rate, & Track Number

Media Type	Format	Drive Type	PC Type Pins	Select Drive Type	Set Perpendicular Mode	DRR	FM Bit
APPLE MODE							
1MByte	(MFM)	Horizontal	11	00	00	10 or 01	1
2MByte	(MFM)	Horizontal	11	00	00	00	1
4MByte	(MFM)	Horizontal		INVALID	CONFIGURATION		
13MByte	(MFM)	Horizontal	11	01	00	11	1
1MByte	(MFM)	Perpendicular	11	00	01	10	1
2MByte	(MFM)	Perpendicular	11	00	01	00	1
4MByte	(MFM)	Perpendicular	11	00	11	11	1
400K	(GCR)	Horizontal	11	11	00	00	0
800K	(GCR)	Horizontal	11	11	00	00	0
400K	(GCR)	Perpendicular	11	11	01	00	1
800K	(GCR)	Perpendicular	11	11	01	00	1
PS/2 MODE							
1MByte	(MFM)	Horizontal	00	00	00	10 or 01	1
2MByte	(MFM)	Horizontal	00	00	00	00	1
4MByte	(MFM)	Horizontal		INVALID	CONFIGURATION		
13MByte	(MFM)	Horizontal	00	01	00	11	1
1MByte	(MFM)	Perpendicular	00	00	01	10	1
2MByte	(MFM)	Perpendicular	00	00	01	00	1
4MByte	(MFM)	Perpendicular	00	00	11	11	1
PC/AT MODE							
1MByte	(MFM)	Horizontal	01	00	00	10 or 01	1
2MByte	(MFM)	Horizontal	01	00	00	00	1
4MByte	(MFM)	Horizontal		INVALID	CONFIGURATION		
13MByte	(MFM)	Horizontal	01	01	00	11	1
1MByte	(MFM)	Perpendicular	01	00	01	10	1
2MByte	(MFM)	Perpendicular	01	00	01	00	1
4MByte	(MFM)	Perpendicular	01	00	11	11	1
GENERAL MODE							
1MByte	(MFM)	Horizontal	10	00	00	10 or 01	1
2MByte	(MFM)	Horizontal	10	00	00	00	1
4MByte	(MFM)	Horizontal		INVALID	CONFIGURATION		
13MByte	(MFM)	Horizontal	10	01	00	11	1
1MByte	(MFM)	Perpendicular	10	00	01	10	1
2MByte	(MFM)	Perpendicular	10	00	01	00	1
4MByte	(MFM)	Perpendicular	10	00	11	11	1
400K	(GCR)	Horizontal	10	11	00	00	0
800K	(GCR)	Horizontal	10	11	00	00	0
400K	(GCR)	Perpendicular	10	11	01	00	1
800K	(GCR)	Perpendicular	10	11	01	00	1

Table 1.4.1.2. Selecting Floppy Drive Types

1.4.2 PS/2 Mode

Under PS/2 mode, all registers, which have the same functions as that in

IBM PS/2, are available. The supported formats are MFM and FM recording formats to be supported by the world wide standard FDC µPD765A. As for the commands, the FDC can support the all commands except the following commands, which should be disclosed to Apple Computer only:

- Format/Write	- Disable/Enable DPLL	- Eject Disk
- Set Drive Mode	- Set Motor Control	- Raw Dump

As for the Data Rates, the bits (DRATE1, DRATE0) in the Data Rate Register or the bits (DRATE1, DRATE0) in the Configuration Control Register should be set. If one register is set and then the other register is set, the register that was set last has the priority.

As for the target drive, the bits (DS1, DS0) in the Digital output Register can automatically select the desired drive so that the polling function can not be supported.

As for the formats, the (FM) bit in the issued commands can automatically select either FM or MFM formats.

As for turning the FDD motor On of Off, the bits (EM3, EM2, EM1, EM0) in the Digital output Register should be used.

As for the value of the preshifted Write Data signal, the bits (PCS2, PCS1, PCS0) in the Data Rate Register should be defined and the cylinder to be written with the preshifted Write Data signal should be defined by the PRETRK bits in the Configure command. The reset default of this PRETRK bits is set to the zero so that every cylinder is written with the preshifted Write Data signal.

On the other hand, the Data Register with FIFO can always be available in the only Execution phase of the Read/Write commands group after the EFO bit and the FIFOTHD bits in the Configure command are set.

The combination of Select Drive Type and Perpendicular Mode commands, in conjunction with the setting of the proper bits in the Data Rate Register (DRR) register are used to select the types Floppy Disk Drive to be used. Selection can be one of the following drives; 2DD, 2HD, 2ED, 2TD and GCR. Please refer to Table 1.4.1.2.

1.4.3 PC/AT Mode

Under PC/AT mode, the following registers, which have the same

functions as that in IBM PC/AT/, are available;

- Status resister (STR)
- Data register (DTR)
- Data Rate Register (DRR)
- Digital output register (DOR)
- Digital Input register (DIR)
- Configuration Control register (CCR)
- Tape Drive Register (TDR)

Status A, B register are not available in this mode.

As for the supported formats, MFM and FM recording formats as same as that supported by the world wide standard FDC μPD765A are can be supported.

As for the commands, the FDC can support the all commands except the following commands, which should be disclosed to Apple Computer only:

- Format/Write
- Disable/Enable DPLL
- Eject Disk
- Set Drive Mode
- Set Motor Control
- Raw Dump

As for the Data Rates, the bits (DRATE1, DRATE0) in the Data Rate Register or the bits (DRATE1, DRATE0) in the Configuration Control Register should be set. If one register is set and then the other register is set, the register that was set last has the priority.

As for the target drive, the bits (DS1, DS0) in the Digital output Register can automatically select the desired drive so that the polling function can not be supported.

As for the formats, the (FM) bit in the issued commands can automatically select either FM or MFM formats.

As for turning the FDD motor On or Off, the bits (EM3, EM2, EM1, EM0) in the Digital output Register should be used.

As for the value of the preshifted Write Data signal, the bits (PCS2, PCS1, PCS0) in the Data Rate Register should be defined and the cylinder to be written with the preshifted Write Data signal should be defined by the PRETRK bits in the Configure command. The reset default of this PRETRK

bits is set to the zero so that every cylinder is written with the preshifted Write Data signal.

On the other hand, the Data Register with FIFO can always be available in the only Execution phase of the Read/Write commands group after the EFO bit and the FIFOTHD bits in the Configure command are set.

The combination of Select Drive Type and Perpendicular Mode commands, in conjunction with the setting of the proper bits in the Data Rate Register (DRR) register are used to select the types Floppy Disk Drive to be used. Selection can be one of the following drives; 2DD, 2HD, 2ED, 2TD and GCR. Please refer to Table 1.4.1.2.

1.4.4 General Mode

Under General mode, the following registers are available:

- Status resister (STR)
- Data register (DTR)
- Data Rate Register (DRR)

The IBM PS/2 and PC/AT registers are not available.

As for the supported formats, MFM and FM recording formats as same as that supported by the world wide standard FDC µPD765A are can be supported.

As for the commands, the FDC can support the all commands except the following commands, which should be disclosed to Apple Computer only:

- Format/Write	- Disable/Enable DPLL	- Eject Disk
- Set Drive Mode	- Set Motor Control	- Raw Dump

As for the Data Rates, the bits (DRATE1, DRATE0) in the Data Rate Register should be set.

As for the target drive, the bits (DR1, DR0) in the issued commands can automatically select the desired drive so that the polling function can be available.

As for the formats, the (FM) bit in the issued commands can automatically select either FM or MFM formats.

The control to turn the FDD motor On or Off can not be supported.

As for the value of the preshifted Write Data signal, the bits (PCS2, PCS1, PCS0) in the Data Rate Register should be defined and the cylinder to be written with the preshifted Write Data signal should be defined by the PRETRK bits in the Configure command. The reset default of this PRETRK bits is set to the zero so that every cylinder is written with the preshifted Write Data signal.

On the other hand, the Data Register with FIFO can always be available in the only Execution phase of the Read/Write commands group after the EFO bit and the FIFOTHD bits in the Configure command are set.

The Select Capacity command can be used to select the types of drives, 2DD, 2HD, 2ED, 2TD except GCR. Please refer to Table 1.4.1.2.

1.5 Data Transfer Modes

The FDC has the three phases according to the internal operating state in the FDC. One is the Command phase to set the required parameter into the FDC, second is the Execution phase to be performing the issued command and final is the result phase to inform of the host about the result for the executed command.

In these phases, the ways to transfer data between this FDC and the host are the following data transfer modes.

1) DMA transfer mode;

   This transfer mode can be used in the only Execution phase.

2) Non DMA transfer mode;

   This transfer mode, maybe called as the Programmed I/O mode, can be used in all phases but mainly in only Command and Result phases.

Chapter 2 Pin Functions

2.1 Host Interface Pins

Symbol	I/O	Signal Function
RESET	In	RESET. Sets FDC to idle state.
XA1,XA2	In	CRYSTAL INPUTS. For internal oscillator frequency control, a crystal resonator is connected to XA1 and XA2. For external clock input at XA1, XA2 are open. Frequency=24MHz. Supported data transfer rates 1Mbps, 500Kbps, 300Kbps and 250Kbps.
XB	In	TTL EXTERNAL CLOCK INPUT. Frequency =15.6672MHz, for GCR FDD. Frequency =20MHz, for 13Mbyte FDD. When external clock is not supplied, XB pin must be connected to ground.
CS_b	In	CHIP SELECT. Validates RD_b and WR_b signals.
D0-D7	I/O	DATA BUS. Bidirectional three-state data bus with 12mA drive.
A0-A2	In	ADDRESS 0-2. Selects a register in FDC.

A2	A1	A0	R/W	Register
0	0	0	R	Status Register A (SRA)
0	0	1	R	Status Register B (SRB)
0	1	0	R/W	Digital Output Register (DOR)
0	1	1	R/W	Tape Drive Register(TDR)
1	0	0	R	Status Register (STR)
1	0	0	W	Data Rate Register (DRR)
1	0	1	R/W	Data Register with FIFO (DATA)
1	1	0	-	Reserved
1	1	1	R	Digital Input Register (DIR)
1	1	1	W	Configuration Control register (CCR)

Symbol	I/O	Signal Function

RD_b	In	READ DATA. This Control signal causes the host to read data from FDC to the data bus.
WR_b	In	WRITE DATA. This Control signal causes the host to write data from the data bus to the FDC.
DMARQ	Out	DMA REQUEST. Requests data transfer in DMA mode. Normally active high, but in PC/AT™ Mode,this signal goes to high impedance when the D3 bit of DOR is 0.
DMAAK_b	In	DMA ACKNOWLEDGE .Enables DMA cycle. Normally active low, but in PC/AT™ Mode, this signal is disabled when the D3 bit of DOR is 0.
TC	In	TERMINAL COUNT. Terminates data transfer.TC is accepted only while DMAAK_b is active. TC is active high in PC/AT™ Mode and Apple/general Mode,and active low in PS/2™ Mode. Note: If TC signal is not used as an input signal at the completion of the command, the Abnoraml Termination will be set (ST0 = 40) and End of Cylinder will be set (ST0 = 80). Also, see 3.1.9 Status Register 0 and 3.1.10 Status Register 1.
INT	Out	INTERRUPT REQUEST. Requests host to process transferred data and execution results. Normally active high,but in PC/AT™ Mode,this signal goes to high impedance when the D3 bit of DOR is 0.
PCTYP0, PCTYP1	In	PC TYPE PINS. Selects host interface mode.

PCTYP1	PCTYP0	Host I/F Mode	I/F Registers
0	0	PS/2™ Mode	All Registers
0	1	PC/AT™ Mode	DOR, TDR, STR,DRR, DATA,CCR
1	0	General Mode	DATA,STR, DRR
1	1	APPLE Mode	DATA, STR, DDR

2.2 FDD Interface Pins (All outputs have 48mA drive capability)

Symbol	I/O	Signal Function
DS0-DS3_b	Out	DRIVE SELECT. Selects up to four standard FDDs.
ME0_b,ME1_b	Out	MOTOR ENABLE. Controls the MFM FDD spindle motor on/off ; also can be used as a general-purpose
ENBL0_b /ME2_b, ENBL1_b /ME3_b	Out	DRIVE ENABLE. In Apple mode Enable 0,1 enables all communication with the Apple FDD. In other modes Motor Enable Controls the MFM FDD spindle motor on/off.
SEL/HDLD_b CA0/DIR_b CA1/STEP_B CA2/SIDE_B	Out	SELECT/HEAD LOAD, CA0/DIR_b, CA1/STEP_b, CA2/SIDE_B. Multiplexed signals defined as follows: In Apple mode: SELECT_B COMMAND ADDRESS 0-2 These lines are used for 2 reasons in Apple Mode: 1) To multiplex status to RDATA LINE during a Read operation, and 2) To select addressable latches on the Disk Drive during a command operation. In other modes: HEAD LOAD. Sets drive head in the load state. DIRECTION. Specifies the seek direction. <u>DIR</u> <u>Direction</u> 0 Inward 1 Outward STEP PULSE. Generates seek pulses. SIDE. Selects double-sided drive head. <u>SIDE</u> <u>Drive Head</u> 0 Head 1 1 Head 0
LSTRB	Out	LINE STROBE. In Apple mode, this line is used to send a command to the drive.

Symbol	I/O	Signal Function
WDATA_b	Out	WRITE DATA. Write Data and Clock bits to FDD.
WGATE_b	Out	WRITE GATE. Requests FDD to write data.
WPRT_b (*)	In	WRITE PROTECT. Indicates medium is write-protected.
RDATA_b	In	READ DATA. Read data and clock bits from FDD.
DEN0_b (*), DEN1_b (*)	Out	DENSITY. Specifies the density of a drive that can support more than one density. The output is a value corresponding to the selected data transfer rate.
INDEX_b (*)	In	INDEX PULSE. Indicates drive head is positioned at physical start point of track on the medium.
TRK0_b (*)	In	TRACK 0. Indicates drive head is positioned at cylinder 0.
DKCG_b (*) /READY_b (*)	In	DISK CHANGE/READY. Indicates drive status. ENDKCG — DKCG/READY 0 — DKCG 1 — READY
ENDKCG_b (*)	In	ENABLE DISK CHANGE. Enables the disk change signal (DKCG).
DRV2_b (*)	In	DRIVE 2. Indicates whether a second drive is installed and is reflected in Status register A (SRA).

(*) = Indicates Standard (non-Apple) FDD interface signal

2.3 Analog PLL Signals

Symbol	I/O	Signal Function
LPF1, LPF2	Out	LOW PASS FILTER. Phase difference of main PLL devices.
CGP1,CGP2	Out	CHARGE PUMP. Phase difference of sub PLL devices.

2.4 Other Pins

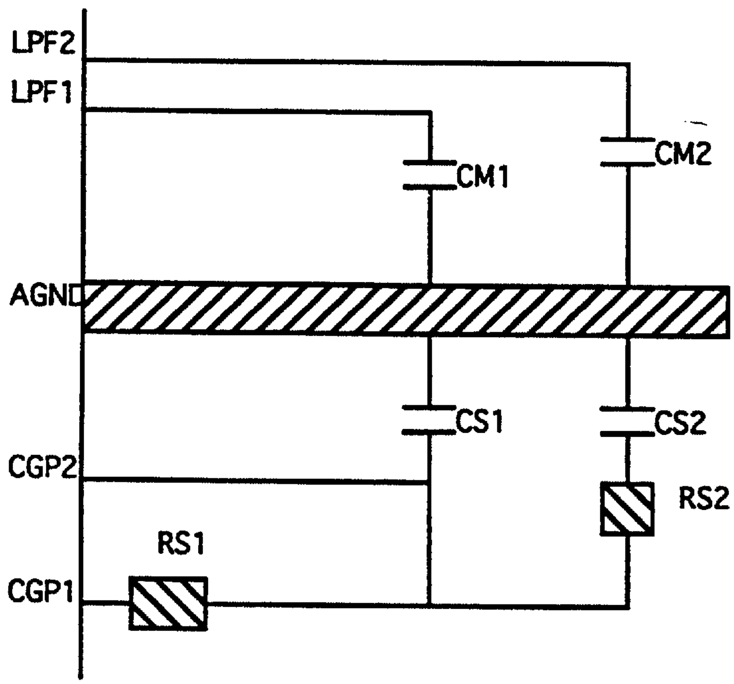
Symbol	I/O	Signal Function
DVDD	-	DIGITAL VDD. +5-volt power for digital circuits.
DGND	-	DIGITAL GROUND. Ground for digital circuits.
BGND	-	BUFFER GROUND. Ground for high current drivers.
AVDD	-	ANALOG VDD. +5-volt supply for analog PLL.
AGND	-	ANALOG GROUND. Ground for analog PLL.
The following four pins are used for the Boundary Scan circuit:		
TCK	I	Clock Input
TDI	I	Data Input
TMS	I	Used to select modes in this test circuit
TDO	O	Data Output

2.5 Output Pin Reset Status

Pin	Reset Status	
D0-D7	INPUT	
DMARQ, INT	In PC/AT™ Mode: In other modes :	HIGH IMPEDANCE LOW

LPF1,LPF2, CGP1,CGP2	UNDEFINED
DS0-DS3, ME0, ME1, ENBL0/ME2, ENBL1/ME3, WDATA, WGATE, SEL/HDLD, CA0/DIR, CA1/STEP, CA2/SIDE, LSTRB	HIGH IMPEDANCE
DEN0, DEN1	Depends on the data transfer rate.

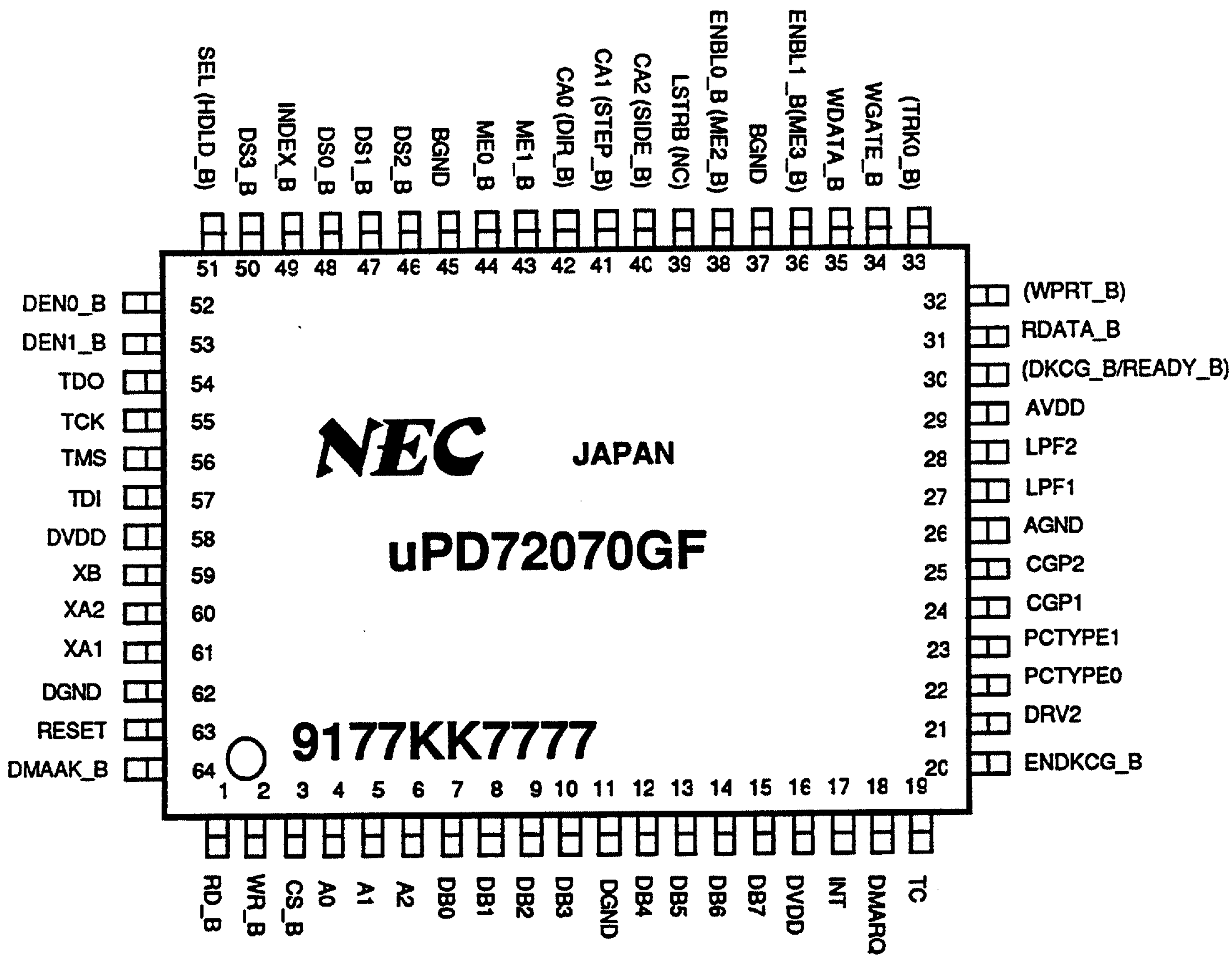
2.6 Recommended Filter Parameters



RS1 = 6.8K
RS2 = 1.0K
CS1 = 1,800pF
CS2 = 22,000pF
CM1 = 4,700pF
CM2 = 68,000pF

Note: The value on CM1 & CM2 sometimes will be required to adjust depending on user's machine.

2.7 Pin Connection Diagram



( ): For Standard Modes Only

_B: Active Low Pins

Chapter 3 Internal Configuration

3.1 Registers

These following registers are available on the FDC. The Status Registers (STR) may contain one of five (5) different register contents. On the resultant phase of commands, it may contain the value for ST0, ST1, ST2, or ST3. Please refer to the specific command for this information.

REGISTERS

1) Status resister (STR)
2) Data register (DTR)
3) Data Rate Register (DRR)
4) PS/2 (TM) register set
    - 4-1) Status A register (SRA)
    - 4-2) Status B register (SRB)
    - 4-3) Digital output register (DOR)
    - 4-4) Digital Input register (DIR)
    - 4-5) Configuration Control register (CCR)
5) Tape Drive Register (TDR)

STATUS REGISTERS (Available only on the Result Phase)

6) Status 0 resister (ST0)
7) Status 1 resister (ST1)
8) Status 2 resister (ST2)
9) Status 3 register (ST3)

Under Apple mode, only 3 registers are available: the Status Register (STR), Data Register (DTR) and Data Rate Register (DRR). Table 3.1 shows how to select a register by setting address signals under an operation mode.

Table 3.1 Register Selection under Operation Modes

Mode	PCTYP1	PCTYP0	CS	A2	A1	A0	R/W	Register
Apple	1	1	0	1	0	0	W	Data Rate Register
	1	1	0	1	0	0	R	Status Register
	1	1	0	1	0	1	W/R	Data Register
PS / 2	0	0	0	0	0	0	R	Status A Register
	0	0	0	0	0	1	R	Status B Register
	0	0	0	0	1	0	R/W	Digital Output Register
	0	0	0	0	1	1	W/R	Tape Drive Register
	0	0	0	1	0	0	W	Data Rate Register
	0	0	0	1	0	0	R	Status Register
	0	0	0	1	0	1	W/R	Data Register
	0	0	0	1	1	1	W	Config. Cntl. Register
	0	0	0	1	1	1	R	Digital Input Register
PC / AT	0	1	0	0	1	0	R/W	Digital Output Register
	0	1	0	0	1	1	W/R	Tape Drive Register
	0	1	0	1	0	0	W	Data Rate Register
	0	1	0	1	0	0	R	Status Register
	0	1	0	1	0	1	W/R	Data Register
	0	1	0	1	1	1	W	Config. Cntl. Register
	0	0	0	1	1	1	R	Digital Input Register
General	1	0	0	1	0	0	W	Data Rate Register
	1	0	0	1	0	0	R	Status Register
	1	0	0	1	0	1	W/R	Data Register
	X	X	1	X	X	X	-	No registers accessed

3.1.1 Status Resister (STR)

Apple Mode

No.	Bit Name	Symbol
D7	Request for Master	RQM
D6	Data input/Output	DIO
D5	Execution mode	EXM
D4	FDC busy	CB
D3	Drive 1 Installed	D1I
D2	Drive 0 Installed	D0I
D1	FDD 1 Busy	D1B
D0	FDD 0 Busy	D0B

Standard Mode

No.	Bit Name	Symbol
D7	Request for Master	RQM
D6	Data input/Output	DIO
D5	Execution mode	EXM
D4	FDC busy	CB
D3	FDD 3 Busy	D3B
D2	FDD 2 Busy	D2B
D1	FDD 1 Busy	D1B
D0	FDD 0 Busy	D0B

Fig. 3.1.1 Bit Function in the Status Register

This register is a Read Only register. The function of this register is changed depending on the operation mode.

<u>UNDER APPLE MODE:</u>

RMQ: This bit indicates the ready state to transfer data for host. Depending on the DIO bit state, RQM bit is set as follows:

When DIO=0;

The host sends data to FDC. When the host writes data into the FDC, RQM bit is reset to 0. When FDC receives this data, RQM bit is set to a high(1).

When DIO=1;

FDC sends data to the host. When FDC sets data in the Data Register, RQM bit is set to a high (1). When the host reads this data from the Data register, RQM bit is reset to 0.

DIO: This bit indicates the direction of the data transferred between the host and the FDC. When this bit is reset as 0, data is transferred from the host to the FDC. When this bit is set as a high (1), data is transferred from the FDC to the host.

EXM: This bit indicates that data is being transferred by using the Non-DMA mode during the Execution phase. This bit is reset during the command phase.

CB: This bit indicates that the FDC is in the command phase, the execution phase if the read/write groups commands or the result phase. When this bit is set, no commands should be written to the Data Register.

D1I: This bit indicates a second floppy disk drive is installed in the system.

D0I: This bit indicates the first floppy disk drive is installed in the system.

D1B: This bit indicates the the Seek Group commands are being performed on the second drive or a Seek Operation termination interrupt is pending. Read/Write commands must not be issued when this bit is active.

D1B: This bit indicates the the Seek Group commands are being performed on the first drive or a Seek Operation termination interrupt is pending. Read/Write commands must not be issued when this bit is active.

UNDER STANDARD MODES:

RMQ: This bit indicates the Ready state to transfer data for host. Depending on the DIO bit state, RQM bit is set as follows:

When DIO=0;

The host sends data to FDC. When the host writes data into the FDC, RQM bit is reset to 0. When FDC receives this data, RQM bit is set to a high(1).

When DIO=1;

The FDC sends data to the host. When FDC sets data in the Data Register, the RQM bit is set to a high (1). When the host reads this data from the Data Register, RQM bit is reset to 0.

DIO: This bit indicates the direction of the data transferred between the host and the FDC. When this bit is reset as 0, data is transferred from the host to the FDC. When this bit is set as a high(1), data is transferred from the FDC to the host.

EXM: This bit indicates that data is being transferred by using the Non-DMA mode during the Execution phase. This bit is reset during the command phase.

CB: This bit indicates that the FDC is in the command phase, the execution phase if the read/write groups commands or the result phase. When this bit is set, no commands should be written to the Data Register.

D3B: This bit indicates the the Seek Group commands is being performed on the fourth drive or a Seek Operation termination interrupt is pending. Read/Write commands must not be issued when this bit is active.

D2B: This bit indicates the the Seek Group commands is being performed on the third drive or a Seek Operation termination interrupt is pending. Read/Write commands must not be issued when this bit is active.

D1B: This bit indicates the the Seek Group commands is being performed on the second drive or a Seek Operation termination interrupt is pending. Read/Write commands must not be issued when this bit is active.

D0B: This bit indicates the the Seek Group commands is being performed on the first drive or a Seek Operation termination interrupt is pending. Read/Write commands must not be issued when this bit is active.

3.1.2 Data Register (DTR)

This register consists of programmable length data FIFO with a maximum length of 16-bytes for data. Commands are also sent to this register but only one command byte is stored at one time.

3.1.3 Data Rate Register (DRR)

No.	Bit Name	Symbol
D7	Resets by Software	S/W RST
D6	enters standby mode	STDBY
D5	reserved	-
D4	sets values for precompensation	PCS2
D3		PCS1
D2		PCS0
D1	sets Data rate	DRATE1
D0		DRATE0

Fig. 3.1.3.1 Bit function

This Write Only register is available under any operation mode.

S/WRST: When this bits is set high (1), the FDC enters into the reset condition. This bit is automatically reset by itself.

STDBY: When this bit is set high (1), the FDC enters into the power down mode. In power down mode, all circuits are turned off. The FDC will terminate this mode after the reset condition, or when any register is read or written by the host.

PCS2-0: These bits select the preshift value of the write precompensator the FDC will use on the WDATA disk interface output. Table 3.1.8.1 shows the values for these bits.

In Apple Mode while recording in GCR, the precompensation value is always set to zero, independent of the bits (PCS2-PCS0) in the DRR register.

Table 3.1.8.1 PCS bits v.s. Preshift values

			2ED/2HD/2DD	2TD	
PCS2	PCS1	PCS0	Value(ns)	Value(ns)	
0	0	0		Reset default	
0	0	1	41.7	50.0	
0	1	0	83.3	100.0	
0	1	1	125.0	150.0	Apple's MFM value
1	0	0	166.7	200.0	
1	0	1	208.3	Not used	
1	1	0	250.0	Not used	
1	1	1	0.0	0.0	

Table 3.1.8.2 preshift values after reset condition

	2ED/2HD/2DD	2TD
Data Rate(kbps)	value(ns)	value(ns)
1000	41.7	-
500	125.0	-
300	125.0	-
250	125.0	-
1250	-	50.0

DRATE1-0: These bits determine the data rate to be used. The data rates for MFM format are shown in Table 3.1.8.3. For FM format, the data rates become a half of the shown values in this figure. For data rates under Apple mode, these bits should be set as (DRATE1, DRATE0) = (0,0) or (DRATE1, DRATE0)=(1,1).

Table 3.1.8.3 DRATE bits v.s. Data Rates

DRATE1	DRATE0	Data rate(kbps)	
0	0	500/489.6	
0	1	300	
1	0	250	(Reset default)
1	1	1000/1250	(1000kbps is for 2ED media, 4MB) (1250kbs is for 2TD media; 13MB)

3.1.4 Status Register A (SRA)

No.	Bit Name	Symbol
D7	Pending Interrupt	PINT
D6	Installed drive 2	DRV2_B
D5	Step signal	STEP
D4	Track 0 signal	TRK0_B
D3	Side select signal	SIDE
D2	Index signal	INDEX_B
D1	Write protect signal	WPRT_B
D0	Direction signal	DIR

Fig. 3.1.4 SRA Bit Function

This Read Only register is available under Standard Modes only.

Symbol	Active Level	Description
PINT	High	Reflects the state of the INT pin.
DRV2_B	Low	Reflects if a second drive has been installed or not.
STEP	High	Reflects the state of the STEP_B pin in the drive interface.
TRK0_B	Low	Reflects the state of the TRK0_B pin in the drive interface.
SIDE	High	Reflects the state of the SIDE pin in the drive interface.
INDEX_B	Low	Reflects the state of the INDEX_B pin in the drive interface.
WPRT_B	Low	Reflects the state of the WPRT_B pin in the drive interface.
DIR	High	Reflects the state of the DIR pin in the drive interface.

3.1.5 Status Register B (SRB)

No.	Bit Name	Symbol
D7	reserved	1
D6	reserved	1
D5	Drive Select0	DS0
D4	Write Data signal	WDATA
D3	Read Data signal	RDATA
D2	Write Gate signal	WGATE
D1	Motor On 1	MO1
D0	Motor On 0	MO0

Fig. 3.1.5 SRB Bit Function

This Read only Register is available under Standard Modes only.

Symbol	Active Level	Description
DS0	High	Reflects the state of the DS0_B pin in the drive interface.
WDATA	High	Reflects the state of the WDATA_B pin in the drive interface.
RDATA	High	Reflects the state of the RDATA_B pin in the drive interface.
WGATE	High	Reflects the state of the WGATE_B pin in the drive interface.
MO1-0	High	Reflects the state of the ME1-0_B pins in the drive interface.

3.1.6 Digital Output Register (DOR)

No.	Bit Name	Symbol
D7	Enables Motor On 3	EM3
D6	Enables Motor On 2	EM2
D5	Enables Motor On 1	EM1
D4	Enables Motor On 0	EM0
D3	Enables host interface	EHIF
D2	Enables FDC	RST_B
D1	selects drives	DS1
D0		DS0

Fig. 3.1.6 DOR Bit Function

This Write Only register is available under Standard Modes only.

Symbol	Active Level	Description
EM3-0	High	Enable the Motor Enable Signals (ME3-0_B).
EHIF	High	Enables the host interface signals INT, DMARQ, DMAAK_B and TC.
RST_B	Low	Resets the FDC. Setting this bit to a "0" resets the controller. Setting this bit to a "1" enables the controller for operation.
DS1-0:	See Chart	These bits select a floppy disk drive as the target to be read or written. The external Drive Select signals (DS3-0_B) become active according to the EM3-0 bits.

bits in the Digital Output register						external signals from FDC			
EM3	EM2	EM1	EM0	DS1	DS0	DS3_B	DS2_B	DS1_B	DS0_B
0	0	0	0	X	X	1	1	1	1
0	0	0	1	0	0	1	1	1	0
0	0	1	0	0	1	1	1	0	1
0	1	0	0	1	0	1	0	1	1
1	0	0	0	1	1	0	1	1	1

3.1.7 Digital Input Register (DIR)

No.	Bit Name	Symbol
D7	Disk Change	DSKCHG
D6	reserved	-
D5	reserved	-
D4	reserved	-
D3	reserved	-
D2	reserved	-
D1	reserved	-
D0	reserved	-

Fig. 3.1.7 DIR Bit Function

This Read only Register is available under Standard Modes only.

Symbol	Active Level	Description
DSKCHG	High	Reflects the state of the external pin, DKCG/READY_B, when the external pin, ENDKCG_B is set low. If this ENDKCG_B is set high, this register can not be accessed from the host.

3.1.8 Configuration Control Register (CCR)

No.	Bit Name	Symbol
D7	reserved	-
D6	reserved	-
D5	reserved	-
D4	reserved	-
D3	reserved	-
D2	reserved	-
D1	selects data rate	DRATE1
D0		DRATE0

Fig. 3.1.8.1 CCR Bit Function

This Write Only register is available under Standard Modes only.

Symbol	Active Level	Description
DRATE1-0	See Chart	Determines the data rate to be transferred. The data rates for MFM format are shown in Figure 3.1.8.2. For FM format, these data rates become a half of the values shown.

Fig. 3.1.8.2 DRATE bits v.s. Data Rates for MFM format

DRATE1	DRATE0	Data rate(kbps)	
0	0	500	
0	1	300	
1	0	250	(reset default)
1	1	1000/1250	(1000kbps is for 2ED media, 4MB) (1250kbs is for 2TD media, 13MB)

3.1.9 Tape Drive Register (TDR)

No.	Bit Name	Symbol
D7	reserved	-
D6	reserved	-
D5	reserved	-
D4	reserved	-
D3	reserved	-
D2	reserved	-
D1	selects Tape drives	TDS1
D0		TDS0

Fig. 3.1.9 TDR Bit Function

This Read and Write register is available under Standard Modes only.

Symbol	Active Level	Description
TDS1-0:		These bits are not used in this FDC. These bits are necessary for this FDC to be compatible with the INTEL 82077.

3.1.9 Status Register 0 (ST0)

NO.	Bit Name	Symbol
D7:6	Interrupt Code	IC
D5	Seek End	SE
D4	Equipment Check	EC
D3	Not Ready	NR
D2	Head Address	HD
D1	Floppy in	FIN
D0	Drive	DR

Symbol	Active Level	Description
D7-D6	See Chart	Indicates the causes of the INT request

D7	D6	Indicated causes
0	0	Normal termination of command execution
0	1	Abnormal termination of command execution
1	0	Invalid command issued
1	1	Under Apple Mode: /CSTIN state change, floppy media inserted or removed Under standard modes: Indicates a changed status of FDD

D5	High	This bit is set when a seek operation by Seek or Recalibrate command is terminated normally or abnormally
D4	High	Under Apple mode, this bit is set when errors at the FDD occur. Under Standard modes, this bit is set when the TRK0 signal can not be detected within a certain period in execution if the Recalibrate command.

D3	High	Under Apple mode, this bit reflects the /Ready status in the drive interface. Under standard modes, this bit reflects the READY_B pin.
D2	High	This bit indicates the head status at the time of the INT request. This bit is set to zero when Sense Interrupt Status command is executed.
D1	High	Under Apple mode, this bit reflects the /CSTIN status in the drive interface. Under standard modes, this bit indicates the drive number (DR1), as same as the drive select bit (DR1) in the command, at the time of the INT request.
D0	High	Under all modes, this indicates the drive number (DR0), as same as the drive select bit (DR0) in the command, at the time of the INT request.

3.1.10 Status Register 1 (ST1)

No.	Bit Name	Symbol	Function
D7	End of Cylinder	EN	This bit is set when read or write is attempted beyond the last sector specified by the EOT byte. (TC signal is NOT INPUT)
D6	-	-	This bit is always set to zero.
D5	Data Error	DE	Under Apple mode, this bit is set when the checksum error at the ID field or Data field is detected. DD bit (D5) of Status Register (ST2) specifies either ID or Data field.
D4	Overrun	OR	This bit is set when data transfer service by the host is not performed within the specified amount of time at the data transfer.
D3	-	-	This bit is always set to zero.
D2	No Data	ND	1) This bit is set if the sector specified by the IDR can not be detected on the track when any one of the following five commands is executed: - Read Data - Read Deleted Data - Write Data - Write Deleted Data - Scan group commands 2) This bit is set when an ID with no CRC error or no checksum error is

			not detected on the track in the execution of Read ID command. 3) This bit is set when the sector ID and the contents of the specified IDR does not matched at the Read a Track command execution.
D1	Not Writable	NW	This bit is set when the write protect signal is detected by execution of a write group commands.
D0	Missing Address Mark	MA	1)This bit is set when the IDAM can not be found before two index pulses (or the allowable period) are detected by the execution of a command that accesses the ID of the disk. 2)This bit is set when the DAM or DDAM can not be found after the IDAM is found. MD bit of Status register (ST2) is also set at this time.

3.1.11 Status 2 Register (ST2)

No.	Bit Name	Symbol	Function
D7	-	-	This bit is always set to zero.
D6	Control Mark	CM	This bit is set when the DDAM is detected at the Read Data, Read a Track or Scan group commands execution or when the DAM is detected at the Read Deleted Data execution under MFM format.
D5	Data Error in Data field	DD	This bit is set when the checksum error at the Data field is detected.
D4	No Cylinder	NC	When either C byte of ID matches nor $FF, this bit is set together with ND bit of Status register 1 (ST1).
D3	Scan Equal Hit	SH	This bit indicates the Equal condition to be occurred at the scan group commands.
D2	Scan Not Satisfied	SN	This bit is set when the condition is not satisfied at the scan group commands.

D1	Bad Cylinder	BC	This bit is set together with the ND bit of Status register 1 (ST1) when the C byte of ID field is $FF.
D0	Missing DAM	MD	This bit is set when the Data Address Mark (DAM) or DDAM can not be found after the IDAM is found.

3.1.12 Status Register 3 (ST3)

Apple Mode

No.	Bit Name	Symbol	Function
D7	2MB/4 MB Media	Media	This bit reflects the /2MB or /4MB media status from the drive.
D6	Write Protect	WP	This bit reflects the /Write protect status from the drive.
D5	Ready	RY	This bit reflects the /Ready status from the drive.
D4	Track 0	T0	This bit reflects the Track0 status from the drive.
D3	2MB-4MB drive	Drive	This bit reflects the 2MB-4MB drive status from the drive.
D2	Mode ID	Mode	This bit reflects the Mode ID status from the drive.
D1	Select media	SelMedia	This bit reflects the Select Media status from the drive.
D0	MFM mode	MFM	This bit reflects the MFM Mode status from the drive.

Standard Modes

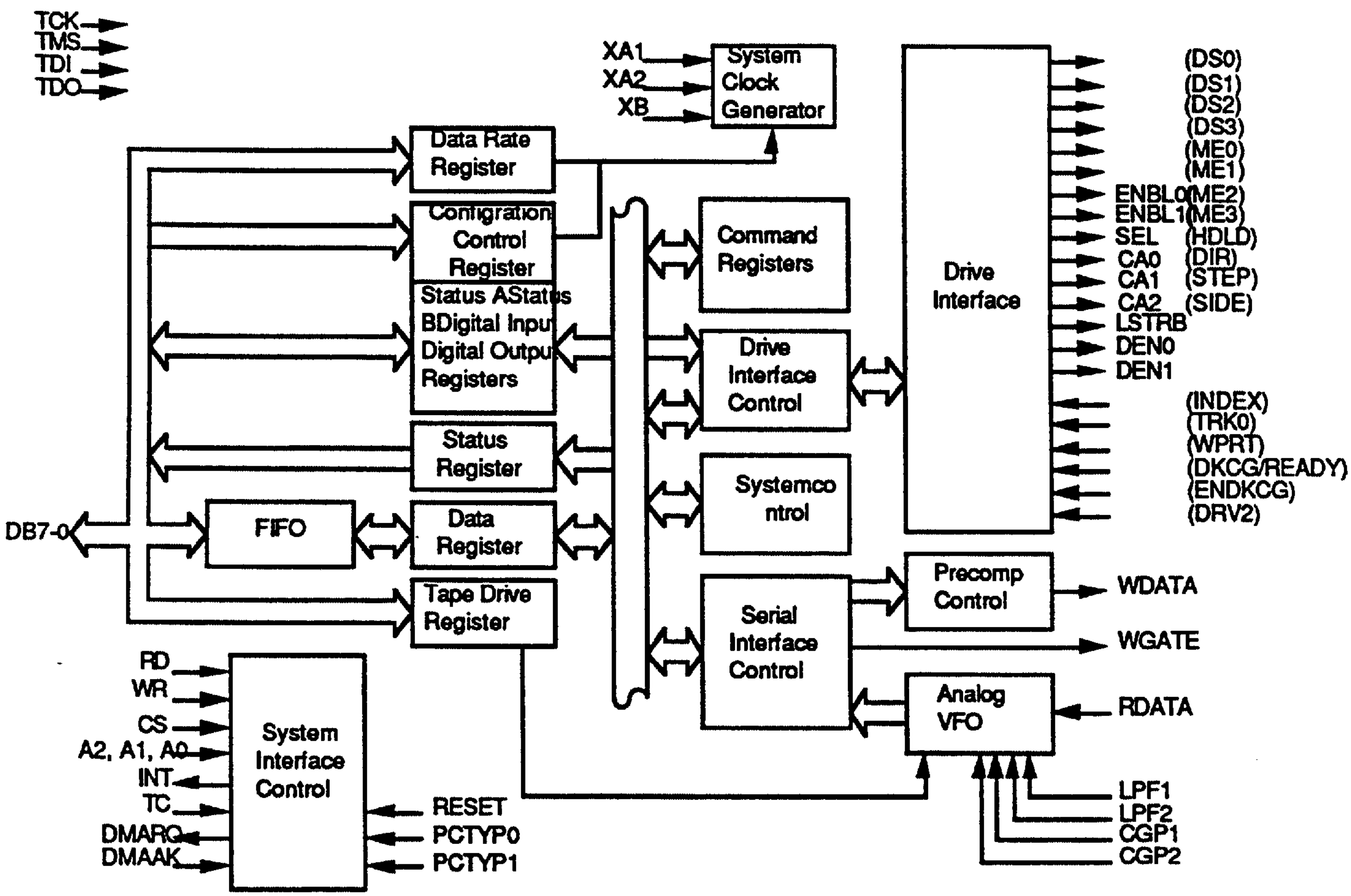
No.	Bit Name	Symbol	Function
D7	Fault	FT	This bit is always set to zero.
D6	Write protect	WP	This bit reflects the WPRT_B pin in the drive interface.
D5	Ready	RY	This bit reflects the READY_B pin in the drive interface.
D4	Track 0	T0	This bit reflects the TRK0_B pin in the drive interface.
D3	Two Side	TS	This bit is always set to high (1).
D2	Head Address	HD	This bit reflects the SIDE_B pin in t

			he drive interface.
D1	Drive Select 1	DR1	This bit reflects the DR1 bit in the issued command.
D0	Drive select 0	DR0	This bit reflects the DR0 bit in the issued command.

3.2 System Interface Control

The block diagram shown in Figure 3.2.1 shows the functional blocks that handle the transfer of data between the host and this FDC.

Fig. 3.2.1 72077 System Block Diagram



( ) : For standard FDD

3.3 Serial Interface Control

This block is used to change data from bytes to serial bits and from serial bits to bytes for the read/write groups commands.

3.4 Drive Interface Control

This block is used to handle the output signals to FDDs and the input signals from FDDs.

3.5 Drive Interface

This block consists of the high current drivers and the receivers for FDD signals.

3.6 Analog PLL

This block generates the Read-clock to be synchronized with the RDATA signal from FDD.

3.7 System Clock Generator

This block generates the internal clocks required for the internal blocks from XA and XB clock source.

3.8 Precompensator Control

This block generates the WDATA signal to be preshifted according to the programmed value. Under GCR mode, this block is always disabled.

Chapter 4 Commands

The following is an explanation of Common Parameters in commands used in the FDC:

FM (Recording Mode Format)

Under Apple mode, the FDC can operate in MFM recording mode when this bit is set 1(high) and the FDC can operate in GCR recording mode when this is set 0(low).

Under Standard modes, the FDC can operate in MFM recording mode when this is set 1(high) and the FDC can operate in FM recording mode when this is set 0(low).

MT (Multi Track)

When this bit is 1(high), the operation to Read or Write for multi tracks is specified.

TB (Tag Byte for GCR recording)

During operations that write data to the FDD, when this is 1(high), the data for the Tag byte field must be transferred from the host to the FDC.

During operations that write data to the FDD, when this is 0(low), the Tag byte field is automatically filled with "0". This does not require any transfer from the host.

During operations that read data from the FDD, when this is 1(high), the Tag byte field is transferred from the FDC to the host.

During operations that read data from the FDD, when this is 0(low), the Tag byte field is not transferred.

SK (SKIP under standard modes)

When this bit is 1(high) and FDC detects the DDAM during operating the Read Data command or when this is 1(high) and FDC detects the DAM during operating the Read Deleted Data command, the data in the data field to be transferred are skipped.

When this bit is 0(low), the data in the data field are transferred.

HD (Head)

Specifies the physical head number. When this bit is 1(high), side 1 is selected and when this is 0(low), side 0 is selected.

DR1,0 (Drive Select)

Specifies the drive number from 0 to 3.

CYLINDER

Indicates the cylinder number

Gap4 is located from the last position of the last sector from the index position.

.Configure

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
command	W	0	0	0	1	0	0	1	1	command code
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFO	POL	FIFOTHR				
	W	PRETRK								
Execution										Sets parameters as specified.

FUNCTION

The host uses this command to set several internal parameters in the FDC.

PARAMETERS

EIS Under only Standard modes, the EIS enables the FDC to perform the Seek command before the FDC performs the Read/Write groups commands without issued Seek command. When EIS is set a high(1), this implied seek function becomes active.

EFO The EFO bit is used to enable the Data FIFO in the FDC. When this EFO is set a low (0), the Data FIFO is enabled. When this EFO is high (1), the Data FIFO is disabled.

POL The POL bits is irrelevant to the FDC operation.

FIFOTHR Once the EFO bit is set a high(1), the FIFOTHR bits is used to determine the threshold of the Data FIFO during the FDC is operating the Read/Write groups commands in the Execution phase. This threshold can be programmed from 1 to 16 bytes.

PRETRK The PRETRK bits are used to specify the track to begin precompensation of the FDD write data .

ERROR CONDITIONS

There are no error condition for this command.

Disable/Enable DPLL

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
command	W	DL	0	0	0	1	0	1	1	command code
	W	X	X	X	X	X	X	X	DR	
Execution										/DPLL sets to specified value

FUNCTION

Under Apple mode only, the effect of this command is to set the /DPLL command bit in the FDD. This disables the integrated Digital Phase Lock Loop (DPLL) in the FDD. The FDC will not handshake this command.

DL = "0" DPLL DISABLED

DL = "1" DPLL ENABLED

ERROR CONDITIONS

This command has no error condition because this command is used only in a development environment.

Dumpreg

Phase	R/W	D7 D6 D5 D4 D3 D2 D1 D0	Remarks
command	W	0 0 0 0 1 1 1 0	command code
Result	R	PCN0	Dumps internal used parameters.
	R	PCN1	
	R	PCN2	
	R	PCN3	
	R	Step Rate | Head Unload time	
	R	Head Load time | ND	
	R	Number of Sectors per Track (or End of Track)	
	R	reserved	
	R	0 EIS EFO POL | FIFOTHR	
	R	PRETRK	

FUNCTION

The host can get the internal parameters to be used in the FDC by using this command. This command can be used under Standard modes.

ERROR CONDITIONS

This command has no error conditions.

Eject Disk

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
command	W	0	1	0	1	0	0	1	0	command code
	W	X	X	X	X	X	X	X	DR	
Execution										Floppy disk is ejected from FDD by asserting /EJECT control signal

FUNCTION

Under Apple mode only, this command is used to programmatically eject the floppy in the selected drive. This is done by writing the /Eject control bit in the specified drive. Immediately after asserting the /Eject command to the FDD, the FDC will issue a normal termination interrupt.

ERROR CONDITIONS

Due to the extremely long time, it takes to execute an Eject command, there is no handshaking done by the FDC. In normal operation, the host will be notified of the completion of the Eject command via an interrupt indicating the change in the /CSTIN status line. This can be used to verify that the media has been properly ejected.

Format A Track

Phase	R/W	D7 D6 D5 D4 D3 D2 D1 D0	Remarks
Command	W	0 FM TB 0 1 1 0 1	command code
	W	X X X X X HD DR1 DR0	
	W	(Bytes/Sector) / Format Byte	
	W	Sectors/Track	
	W	GAP3(MFM) / #Sync Groups(GCR)	
	W	Filler Byte	
Execution			FDC formats the entire track
	R	Status Regisiter 0	status information after this command
	R	Status Regisiter 1	
	R	Status Regisiter 2	
	R	Cylinder(irrelevant)	
	R	Head(irrelevant)	
	R	Sector(irrelevant)	
	R	(Bytes/Sector) / Format Byte	

FUNCTION

This command allows an entire track to be formatted. The host must send new values for the cylinder, head, sector and the number of data bytes, to the FDC for each sector to be formatted during the execution phase of this command. If the FDC is in DMA transfer mode, it will issue four DMA requests per sector for the cylinder, head, sector and the number of data bytes for each formatted sector.

If the FDC is in non-DMA transfer mode, it will issue four interrupts per sector and the host must supply the cylinder, head, sector and the number of data bytes for each formatted sector.

For MFM or FM recording, data is written on the disk after the index hole is detected. But for GCR recording, the write can begin anywhere on the track. The host specifies the format of the track by the parameters passed during the command phase. Tag bytes transfer is controlled by the TB parameter.

PARAMETERS

BYTES/SECTOR This is used as the number of bytes in a sector. For GCR recording, this byte should be either 12H, 22H

or 24H. All these hexidecimal values (12H, 22H or 24H) represent 512 bytes of data and 12 Tag bytes. For MFM recording, see the following;

	Bytes in a sector	
Bytes/Sector(16)	MFM	FM
00	inhibited	128
01	256	256
02	512	512
03	1024	1024
04	2048	2048
05	4096	4096
06	8192	8192

Note *1: GAP3 in this case should be set less than 128bytes.

SECTORS/TRACK — This is used as the number of sectors in a track.

SYNC GROUPS(GCR) / GAP3(MFM)

For GCR recording, this specifies the number of the Self Sync byte group. And for MFM recording, this specifies the number of the bytes in the GAP3.

FILLER BYTE — This byte is written into the data field as the data pattern.

ERROR CONDITIONS

Errors occur under the following conditions:

- The WPRT status becomes active.
- The overrun or underrun occur during the data transfer.
- When utilizing the TC input, it does not meet the correct timing period.

Under Apple mode:

- The /CSTIN status in the drive interface is inactive before this is operated.

Under any mode:

- The Ready status at the drive interface is inactive before this is operated.

Format/Write

Phase	R/W	D7 D6 D5 D4 D3 D2 D1 D0	Remarks
command	W	0 FM TB 0 0 0 0 1	command code
	W	X X X X X HD DR1 DR0	
	W	(Bytes/Sector) / Format Byte	
	W	Sectors/Track	
	W	GAP3(MFM)/# Sync Groups(GCR)	
Execution			track data is passed to FDC as in a write operation
	R	Status Regisiter 0	status information after this command
	R	Status Regisiter 1	
	R	Status Regisiter 2	
	R	Cylinder(irrelevant)	
	R	Head(irrelevant)	
	R	Sector(irrelevant)	
	R	(Bytes/Sector) / Format Byte	

FUNCTION

This command is virtually the same as the Format a Track command with the exception that the filler byte in not specified. Instead, the host transfers the data as in the Write Data command. This capability is required to optimize when writing data and to support GCR recording on perpendicular FDD drives.

This command allows an entire track to be formatted.

The host must send new values for the cylinder, head, sector and the number of data bytes, to the FDC for each sector to be formatted.

PARAMETERS

These parameters are same as that of the Format a Track command.

ERROR CONDITIONS

Errors occur under the following conditions:

- The WRITE PROTECT status is active.
- The overrun or underrun occur during the data transfer.
- Under Standard / Apple modes, the drive interface indicates a NON_READY drive status.

Invalid

In the following two cases, 10(2) (IC: Invalid Command) is set to the Interrupt code (high bits) of ST0, and is set to all remaining bits (ST0=80H).

- When an undefined command code is issued
- When the Sense Interrupt Status command is activated even though an INT request by termination of the seek group commands or by a drive status change is not generated.

Perpendicular Mode

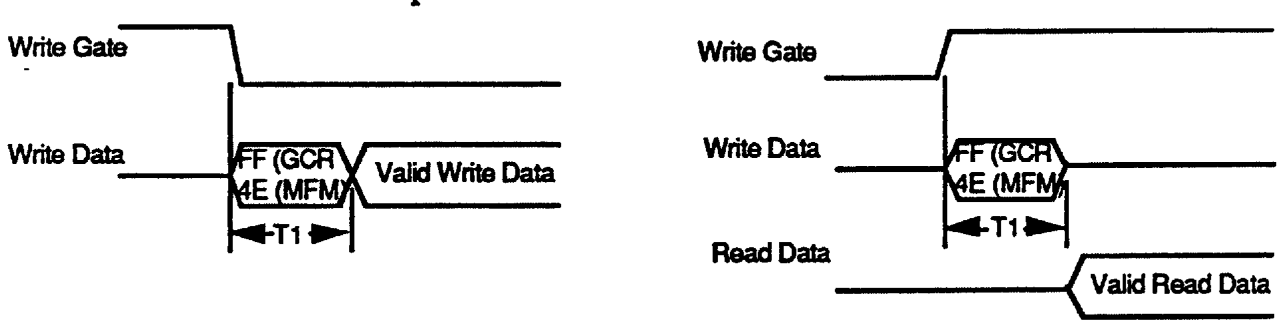
Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
command	W	0	0	0	1	0	0	1	0	command code
command		X	X	X	X	X	X	D1	D0	Echo back for this command.

FUNCTION

The Perpendicular Mode command should be issued prior to executing READ / WRITE / FORMAT commands that access a disk drive with perpendicular recording capability. With this command, the length of the GAP2 field and VCO enable timing can be altered to accommodate the unique requirements of these disk drives. Please refer to the following table for the perferred settings. Selection of the 500 Kbps and 1 Mbps perpendicular modes is independent of the actual data rate selected in the Data Rate register. The User must ensure that the two data rates remain consistent.

D1	D0	MODE	VCO Low Time after INDEX	Length of Gap2 format Field	Portion of Gap2 Written by Write Data Operation	Gap2 VCO Low time / Read Op.
0	0	Conventional Mode	33 Bytes	22 Bytes	0 Bytes	24 Bytes
0	1	Perpendicular Mode 500Kbps	33 Bytes	22 Bytes	19 Bytes	24 Bytes
1	0	RESERVED	33 Bytes	22 Bytes	0 Bytes	24 Bytes
1	1	Perpendicular Mode 1Mbps	18 Bytes	41 Bytes	38 Bytes	43 Bytes

Effects of Perpendicular Mode in GCR and MFM Formats



T1 VALUES

GCR	1MB (MFM)	2MB (MFM)	4MD (MFM)
154 usec	304 usec	304 usec	304 usec

T1 VALUES

GCR	1MB (MFM)	2MB (MFM)	4MD (MFM)
190 usec	190 usec	340 usec	340 usec

Phase	R/W	D7 D6 D5 D4 D3 D2 D1 D0	Remarks
command	W	0 FM 0 1 1 1 1 0	command code
	W	X X X | RDM | HD DR1 DR0	
	W	Cylinder	
	W	Head	
	W	Sector	
	W	Sector Number	
	W	Bytes to dump(MSB)	# of bytes is a 16-bit
	W	Bytes to dump(LSB)	unsigned long integer
Execution			Data is passed back to Host. GCR is returned encoded.
	R	Status Regisiter 0	status information
	R	Status Regisiter 1	after this command
	R	Status Regisiter 2	
	R	Cylinder(irrelevant)	
	R	Head(irrelevant)	
	R	Sector(irrelevant)	
	R	Number of data bytes written(irrelevant)	

FUNCTION

Under Apple mode only, this command supports the following three dump modes:

- Dump from the Index Address Mark
- Dump after the specified ID Address Mark
- Dump after the Data Address Mark

In addition, the FDC begins to transfer data after the FDC is synchronized to the nearest available mark in incoming Data from FDD. After the FDC starts to transfer data, it may be possible for the FDC to lose synchronization with the incoming data because of write splices. If this occurs, meaningless data will be transfered to the host.

The detected mark byte, which the FDC starts to dump data from, is defined under the MFM format that this mark byte is located after the SYNC bytes and the Data and Clock bytes of this mark byte is equal to either $A1 for Data byte and $0A for Clock byte or $C2 for Data byte and $14

for Clock byte.

On the other hand, the detected mark byte is also defined under the GCR format that this mark byte is located after the SYNC bytes and the Data byte of this mark byte is equal to $D5, which is the first data of either Address mark bytes or Data Address mark bytes.

Regarding transfered data under the ONLY MFM FORMAT, the FDC transfers one Data byte and one Clock byte from FDD to the host repeatedly. The host should check what Clock byte has missing clock bits by itself. This transfer is called as the 8 X 8 data transfer and is described later for further detailed. Under the GCR format, the raw data from the FDD should be transfered to the host without denibbling.

1) DUMP FROM INDEX ADDRESS MARK

Under MFM format only, this dumps the requested number of bytes from the track specified, immediately after the Index pulse is input to the FDC and the SYNC bytes are detected and then the Index Address mark, which consists of both the data byte with $C2 and the Clock byte with $14, is detected. The data that is transfered to the host will include the Index address mark itself and the track data according to the rule of the 8 X 8 data transfer.

But under the GCR format, this mode is illegal because the FDD can not output the Index pulse from itself.

When the RDM bits are set to "00", this mode can be entered.

In this mode, the FDC ignores the following errors after the first Address mark is found.

- Read error for CRC for the MFM format
- Read error for Address Mark in the Data field

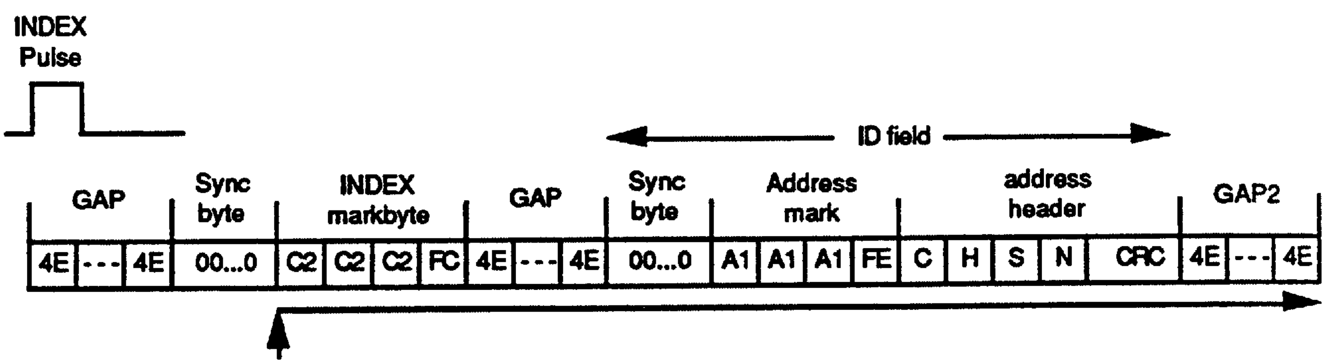


Fig. 4.18.1 Transferred Data for Dump From Index Address Mark

2) DUMP AFTER SPECIFIED ID ADDRESS MARK

When the RDM bits are set to "01", this mode can be entered under the only Apple mode.

This dumps the requested number of bytes from the specified track. Especially under the MFM format, after the FDC finds out the specified ID address mark and then the nearest SYNC bytes, the FDC checks whether the next data after these SYNC bytes is equal to the Mark byte, which is expected as the $A1 for Data byte and the $0A for Clock byte. If this mark is hit, the FDC should start to dump data from and including this Mark byte. But if the Mark byte can not be hit, the FDC changes the expected Data for the Mark byte from the above data to the $C2 for Data byte and the $14 for Clock byte and then the FDC resumes to search the same specified ID field.

After the FDC finds out the specified ID address mark and then the nearest SYNC bytes, the FDC checks whether the next data after these SYNC bytes is equal to the Mark byte, which is expected as the $C2 for Data byte and the $14 for Clock byte. If this mark is hit, the FDC should start to dump data from and including this Mark byte. But if the mark byte can not be hit, the FDC abnormally terminates the command and interrupts to inform to the host this abnormal termination.

For GCR format, after the FDC finds out the specified ID address mark, the FDC is waiting to receive the Mark byte with the $D5 for Data byte. If this mark is hit, the FDC should immediately start to dump data from and including this Mark byte. But if the mark byte can not be hit, the FDC abnormally terminates the command and interrupts to inform to the host this abnormal termination. In addition, the FDC dumps the data without denibblizing the read-data from the FDD.

The Fig. 4. 18. 2 is shown as a example of this mode. In this example, the Data Address mark is located after the specified ID field and the SYNC bytes.

In this dumped mode, the FDC ignores the following errors after the first Address header is found out

- Read error for CRC for the MFM format or Checksum for the GCR format
- Read error for Bit slip byte for the GCR format
- Read error for Address mark in the Data field

Register Name & Bit Symbol Reference

Symbol	Name	Location
-	Reserved	DRR(5)
-	Reserved	ST1(6)
-	Reserved	ST1(6)
-	Reserved	ST2(7)
BC	Bad Cylinder	ST2(1)
CB	FDC Busy	STR(4)
CM	Control Mark	ST2(6)
D0B	Drive 0 Busy	STR(0)
D0I	Drive 0 Installed	STR(2)
D1B	Drive 1 Busy	STR(1)
D1I	Drive 1 Installed	STR(3)
DD	Data Error in Data Field	ST2(5)
DE	Data Error	ST1(5)
DIO	Data Input/Output	STR(6)
DR	Drive	ST0(0)
DRATE0	Data Rate(0)	DRR(0)
DRATE1	Data Rate(1)	DRR(1)
Drive	2MB/4MB Drive	ST3(3)
EC	Equipment Check	ST0(4)
EN	End of Cylinder	ST1(7)
EXM	Execution Mode	STR(5)
FIN	Floppy In	ST0(1)
HD	Head Address	ST0(2)
IC(1)	Interrupt Code(1)	ST0(7)
IC(2)	Interrupt Code(0)	ST0(6)
MA	Missing Address Mark	ST1(0)
MD	Missing Data Mark	ST2(0)
Media	2MB/4MB Media	ST3(7)
MFM	MFM Mode	ST3(0)
Mode	Mode ID	ST3(2)
NC	No Cylinder	ST2(4)
ND	No Data	ST1(2)
NR	Not Ready	ST0(3)
NW	Not Writable	ST1(1)
OR	Overrun	ST1(4)
PCS0	Precompensation(0)	DRR(2)
PCS1	Precompensation(1)	DRR(3)
PCS2	Precompensation(2)	DRR(4)
RQM	Request for Master	STR(7)
RY	Ready	ST3(5)
S/W RST	FDC Software Reset	DRR(7)
SE	Seek End	ST0(5)
SelMedia	Select Media	ST3(1)
SH	Scan Equal Hit	ST2(3)
SN	Scan not Satisfied	ST2(2)
STDBY	Standby Mode	DRR(6)
T0	Track 0	ST3(4)
WP	Write Protect	ST3(6)

8.4.1.2 State Description.

The Behavior of the TAP controller in each of the controller states is briefly described as follows:

Test-Logic-Reset

The JTAG implemented into the FDC is disabled so that normal operation of the FDC system logic can continue unhindered. This is achieved by initializing the instruction register to contain the BYPASS instruction. No matter what the original state of the TAP controller, it will enter Test-Logic-Reset when TMS is held high for at least five rising edges of TCK. The TAP controller remains in this state while TMS is high.

If the TAP controller should leave the Test-Logic-Reset TAP controller state as a result of an erroneous low signal on the TMS line at the time of a rising edge on TCK (for example, a glitch due to external interference), it will return to the Test-Logic-Reset state following three rising edges of TCK with the TMS line at the intended high logic level. The operation of the test logic is such that no disturbance is caused to the FDC logic operation as the result of such an error. On leaving the Test-Logic-Reset controller state, the TAP controller moves into the Run-Test/Idle controller state where no action will occur because the current instruction has been set to select operation of the bypass register. This JTAG logic is also inactive in the Select-DR-Scan and Select-IR-Scan controller states.

Run-Test/Idle

This is a TAP controller state between scan operations. Once entered, the TAP controller will remain in the Run-Test/Idle state as long as TMS is held low. When TMS is high and a rising edge is applied at TCK, the TAP controller moves to the Select-DR-Scan state.

In the Run-Test/Idle controller state, activity in a certain selected instruction occurs only when certain instructions are present.

For instructions that do not cause functions to execute in the Run-Test/Idle controller state, all test data registers selected by the current instruction retains their previous state (i.e., Idle).

The instruction does not change while the TAP controller is in this state.

Select-DR-Scan

This is a temporary controller state in which Boundary -Scan and Bypass registers selected by the current instruction retain their previous state.

If TMS is held low and a rising edge is applied to TCK when the TAP controller is in this state, then the TAP controller moves into the Capture-DR

state and a scan sequence for the selected register is initiated. If TMS is held high and a rising edge is applied to TCK, the TAP controller moves on to the Select-IR-Scan state.

The instruction does not change while the TAP controller is in this state.

Select-IR-Scan

This is a temporary controller state in which Boundary-Scan and Bypass registers selected by the current instruction retain their previous state.

If TMS is held low and a rising edge is applied to TCK when the TAP controller is in this state, then the TAP controller moves into the Capture-IR state and a scan sequence for the Instruction register is initiated. If TMS is held high and a rising edge is applied to TCK, the TAP controller returns to the Test-Logic-Reset state.

The instruction does not change while the TAP controller is in this state.

Capture-DR

In this controller state, data are parallel-loaded into Boundary-Scan registers selected by the current instruction on the rising edge of TCK.

The instruction does not change while the TAP controller is in this state.

When the TAP controller is in this state and a rising edge is applied to TCK, the TAP controller enters either the Exit1-DR state if TMS is held at 1 or the Sift-DR state if TMS is held at 0.

Shift-DR

In this controller state, either Boundary-Scan or Bypass register connected between TDI and TDO as a result of the current instruction shifts data one stage towards its serial output on each rising edge of TCK.

Boundary-Scan and Bypass register that are selected by the current instruction, but are not placed in the serial path, retains their previous state unchanged.

The instruction does not change while the TAP controller is in this state.

When the TAP controller is in this state and a rising edge is applied to TCK, the TAP controller enters either the Exit1-DR state if TMS is held at 1 or remains in the Shift-DR state if TMS is held at 0.

Exit1-DR

This is a temporary controller state. If TMS is held high, a rising edge applied to TCK while in this state causes the TAP controller to enter the Update-DR state, which terminates the scanning process. If TMS is held low and a rising edge si applied to TCK, the TAP controller enters the Pause-DR state.

Boundary-Scan and Bypass registers selected by the current instruction retain their previous state unchanged.

The instruction does not change while the TAP controller is in this state.

Pause-DR

This controller state allows shifting of either Bypass or Boundary-Scan register in the serial path between TDI and TDO to be temporarily halted. These registers selected by the current instruction retain their previous state unchanged.

The TAP controller remains in this state while TMS is low. When TMS goes high and a rising edge is applied to TCK, the TAP controller moves on to the Exit2-DR state.

The instruction does not change while the TAP controller is in this state.

Exit2-DR

This is a temporary controller state. If TMS is held high and a rising edge is applied to TCK while in this state, the scanning process terminates and the TAP controller enters the Update-DR controller state. IF TMS is held low and a rising edge is applied to TCK, the TAP controller enters the Shift-DR state.

Bypass and Boundary-Scan registers selected by the current instruction retain their previous state unchanged.

The instruction does not change while the TAP controller is in this state.

Update-DR

Boundary-Scan register is provided with a latched parallel output to prevent changes at the parallel output while data is shifted in the associated shift-register path in response to certain instructions (e.g., EXTEST). Data is latched onto the parallel output of this register from the shift-register path on the falling edge of TCK in the Update-DR controller state. The data held at the latched parallel output should not change other than in this controller state.

All shift-register stages in Boundary-Scan register selected by the current instruction retain their previous state unchanged.

The instruction does not change while the TAP controller is in this state.

When the TAP controller is in this state and a rising edge is applied to TCK, the TAP controller enters either the Select-DR-Scan state if TMS is held at 1 or the Run-Test/Idle state if TMS is held at 0.

Capture-IR

In this controller state, the shift-register contained in the instruction register loads the pattern (01 binary) of fixed logic values on the rising edge of TCK.

Either Bypass or Boundary-Scan register selected by the current instruction retain their previous state. The instruction does not change while the TAP controller is in this state.

When the TAP controller is in this state and a rising edge si applied to TCK, the TAP controller enters either the Exit1-IR state if TMS is held at 1 or the Shift-IR state if TMS is held at 0.

Shift-IR

In this controller state, the shift-register contained in the instruction register is connected between TDI and TDO and shifts data one stage towards its serial output on each rising edge of TCK.

Either Bypass or Boundary-Scan register selected by the current instruction retain their previous state. The instruction does not change while the TAP controller is in this state.

When the TAP controller is in this state and a rising edge is applied to TCK, the TAP controller enters either the Exit1-IR state if TMS is held at 1 or remains in the Shift-IR state if TMS is held at 0.

Exit1-IR

This is a temporary controller state. If TMS is held high, a rising edge applied to TCK while in this state causes the TAP controller to enter the Update-IR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the TAP controller enters the Pause-IR state.

Either Bypass or Boundary-Scan register selected by the current instruction retain their previous state. The instruction does not change while the TAP controller is in this state and the instruction register retains its state.

Pause-IR

This TAP controller state allows shifting of the instruction register to be halted temporarily.

Either Bypass or Boundary-Scan register selected by the current instruction retain their previous state. The instruction does not change while the TAP controller is in this state and the instruction register retains its state.

The TAP controller remains in this state while TMS is low. When TMS goes high and a rising edge is applied to TCK, the TAP controller moves on to the Exit2-IR state.

Exit2-IR

This is a temporary controller state. If TMS is held high and a rising edge is applied to TCK while in this state, termination of the scanning process results, and the TAP controller enters the Update-IR controller state. If TMS is held low and a rising edge is applied to TCK, the TAP controller enters the Shift-IR state.

Either Bypass or Boundary-Scan register selected by the current instruction retain their previous state. The instruction does not change while the TAP controller is in this state and the instruction register retains its state.

Update-IR

The instruction shifted into the instruction register is latched onto the parallel output from the shift-register path on the falling edge of TCK in this controller state. Once the new instruction has been latched, is becomes the current instruction.

Either Bypass or Boundary-Scan register selected by the current instruction retain their previous state.

When the TAP controller is in this state and a rising edge is applied to TCK, the TAP controller enters the Select-DR-Scan state if TMS is held at 1 or the Run-Test/Idle state if TMS is held at 0.

The Pause-DR and Pause-IR controller states are included so that shifting of data through Bypass, Boundary-Scan or instruction register can be temporarily halted.

8.4.1.3 TAP Controller Operation

The operation of this TAP controller is as follows:

The TAP controller shall only change state in response to the following events: (i) A rising edge of TCK or (ii) Power-up.

The TAP controller generates signals to control the operation of Bypass, Boundary-Scan and instruction registers as defined in this standard (Figs 8.4-3 and 8.4-4).

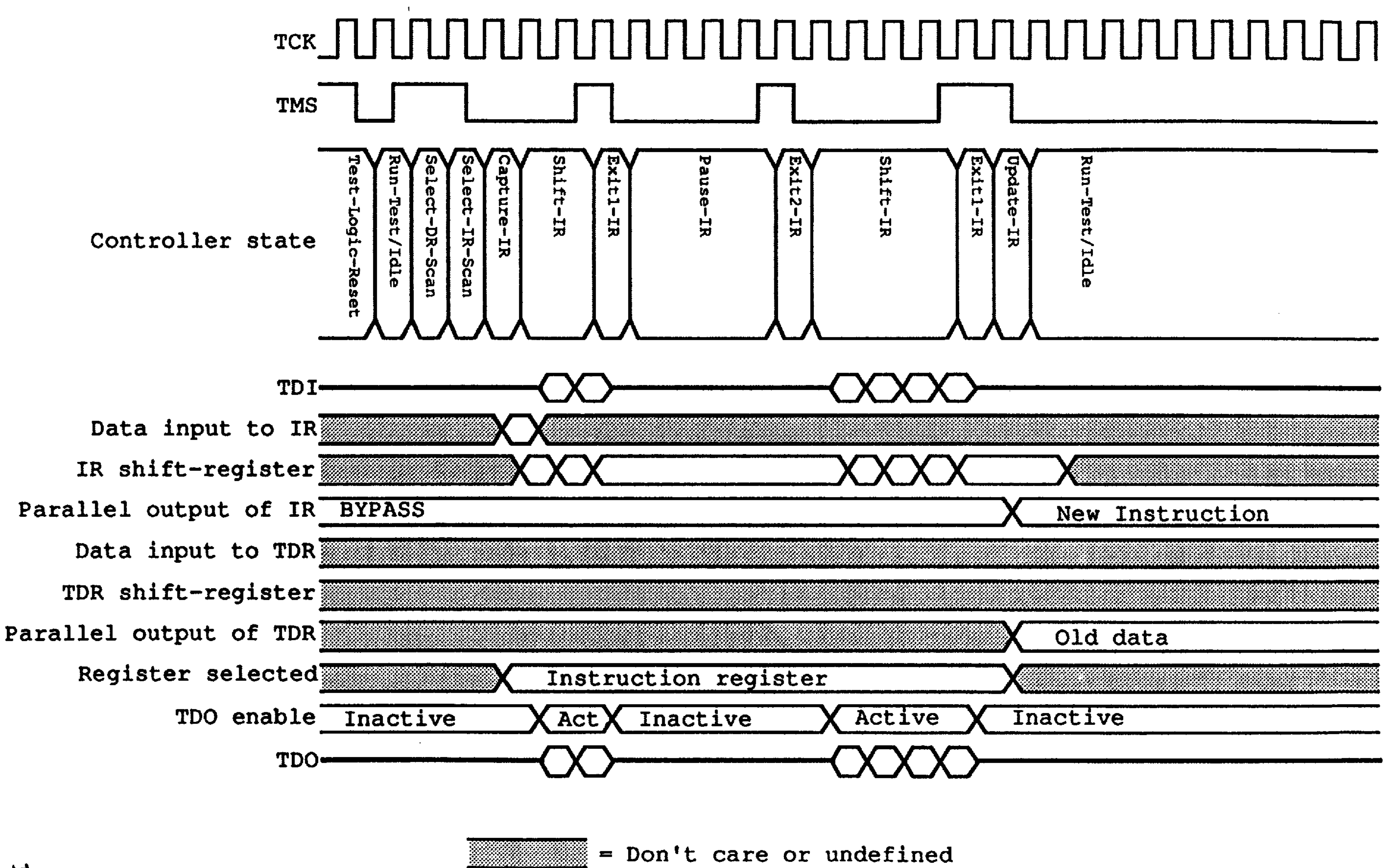
The TDO output buffer and the circuitry that selects the register output fed to TDO are controlled as shown in Table 8.4-1.

Changes at TDO defined in Table 8.4-1 occur on the falling edge of TCK following entry into the state.

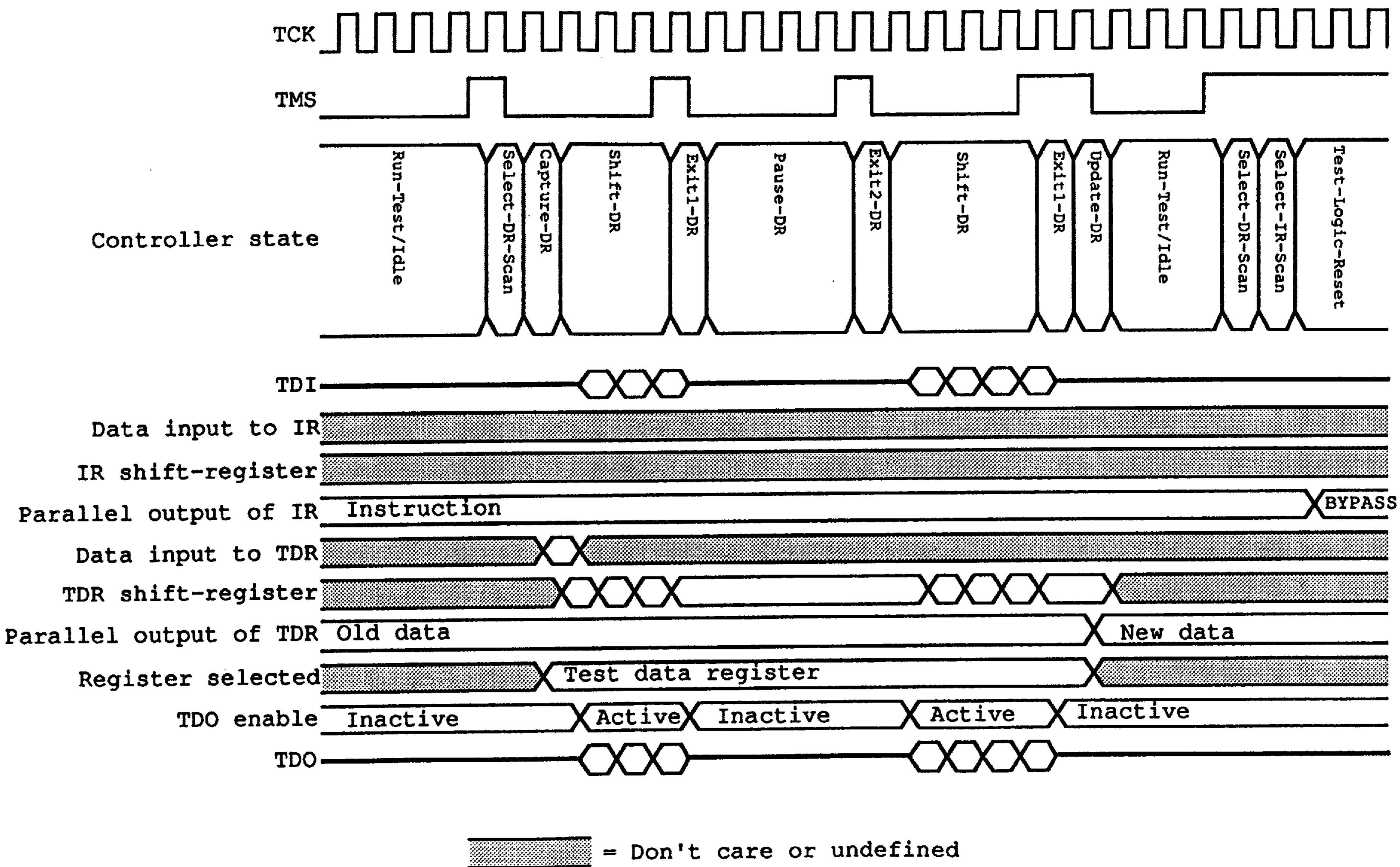
Table 8.4-1 Operation in Each Controller State

Controller State	Register Selected to Drive TDO	TDO Driver
Test-Logic-Reset	Undefined	Inactive
Run-Test/Idle	Undefined	Inactive
Select-DR-Scan	Undefined	Inactive
Select-IR-Scan	Undefined	Inactive
Capture-IR	Undefined	Inactive
Shift-IR	Instruction	Active
Exit1-IR	Undefined	Inactive
Pause-IR	Undefined	Inactive
Exit2-IR	Undefined	Inactive
Update-IR	Undefined	Inactive
Capture-DR	Undefined	Inactive
Shift-DR	Test data	Active
Exit1-DR	Undefined	Inactive
Pause-DR	Undefined	Inactive
Exit2-DR	Undefined	Inactive
Update-DR	Undefined	Inactive

The assignment of controller states in the example implementation is given in Table 8.4.-2 (see the section 8.4.3) .



TCK
TMS
Controller state
Test-Logic-Reset
Run-Test/Idle
Select-DR-Scan
Select-IR-Scan
Capture-IR
Shift-IR
Exit1-IR
Pause-IR
Exit2-IR
Shift-IR
Exit1-IR
Update-IR
Run-Test/Idle
TDI
Data input to IR
IR shift-register
Parallel output of IR
BYPASS
New Instruction
Data input to TDR
TDR shift-register
Parallel output of TDR
Old data
Register selected
Instruction register
TDO enable
Inactive
Act
Inactive
Active
Inactive
TDO
= Don't care or undefined


TCK
TMS
Controller state
Run-Test/Idle
Select-DR-Scan
Capture-DR
Shift-DR
Exit1-DR
Pause-DR
Exit2-DR
Shift-DR
Exit1-DR
Update-DR
Run-Test/Idle
Select-DR-Scan
Select-IR-Scan
Test-Logic-Reset
TDI
Data input to IR
IR shift-register
Parallel output of IR
Instruction
BYPASS
Data input to TDR
TDR shift-register
Parallel output of TDR
Old data
New data
Register selected
Test data register
TDO enable
Inactive
Active
Inactive
Active
Inactive
TDO
= Don't care or undefined

8.4.1.4 TAP Controller Initialization

The initialization for this TAP controller is as follows:

(a) The TAP controller is forced into the Test-Logic-Reset controller state at power-up by the power-on-reset circuitry built into the FDC.

(b) The TAP controller is not initialized by operation of any system input, such as a system reset.

(c) The TAP controller can synchronously enter into the Test-Logic-Reset controller state following five rising edges at TCK (provided TMS is held high).

8.4.2 Instruction Register

As this register is described at the section 8.2, this register is specified by the following;

1) The Instruction shifted into the instruction register is latched such that changes in the effect of an instruction occur only in the Update-IR and the Test-Logic-Reset controller states

2) There is no inversion of data between the serial input and the serial output of the instruction register.

3) This register cell loads a fixed binary "01" pattern data, the 1 into the least significant bit location, in the Capture -IR controller state.

4) This register is set to a fixed binary "01" pattern data, the 1 into the least significant bit location, during the Test-Logic-Reset controller state.

5) When this register is read, the data from the LSB(Least Significant Bit) to the MSB(Most Significant Bit) are output to the TDO pin at each falling edge of the TCK pin.

This JTAG circuitry in this FDC can support the only following three instructions by setting the specified data into this Instruction register:

- Bypass
- Sample/Preload
- Extest

Bits in the Instruction Register

D2	D1	D0	Supported Instructions
0	0	0	EXTEST
0	0	1	Bypass (after the Reset condition)
0	1	0	SAMPLE/PRELOAD
0	1	1	CLAMP-IO

1	0	0	reserved (BYPASS)
1	0	1	reserved (BYPASS)
1	1	0	reserved (BYPASS)
1	1	1	BYPASS

8.4.2.1 Bypass Instruction

This instruction, which is assigned the instruction data "11" or "01", is used to select the only Boundary Scan register for the serial access between the TDI and the TDO pins in the Shift-DR controller state.

When this instruction is selected, the operation of this JTAG circuitry does not effect on the operation of the FDC.

During the Test-Logic-Reset controller state, this Bypass instruction is selected.

8.4.2.2 Sample/Preload Instruction

This instruction, which is assigned the instruction data "10", is used to select the only Boundary Scan register and to have a snap-shot of the normal operation of the FDC to be taken and examined. The data to be had a snap-shot can be latched into the Boundary Scan register.

When this instruction is selected, the JTAG circuitry can operate the following:

1) The operation of this JTAG circuitry does not give effects on the operation of the FDC or on the flow of signals between the FDC pins and the on-chip circuitry.

2) The states of all signals flowing through the FDC pins are loaded into the Boundary Scan register on the rising edge of the TCK pin in the Capture-DR controller state. In this case, the loaded data can not loaded to the input and output pins in the FDC. These only data can be shifted toward the TDO pin in the Shift-DR controller state.

3) Each output bit of the Boundary Scan register can update the data from the old data to the already held data on the falling edge of the TCK pin in the Update-DR controller state. But these data can not be shifted toward the TDO in the Shift-DR controller state.

8.4.2.3 Extest Instruction

This instruction, which is assigned the instruction data "00", also is used to select the only Boundary Scan register for the serial access between the TDI and the TDO pins in the Shift-DR controller state.

When this instruction is selected, the state of all signals driven from system output pins is completely defined by the data shifted into the Boundary-Scan register and change only on the falling edge of TCK in the Update-DR controller state.

When this instruction is selected, the state of all signals received at system input pins is loaded into the Boundary-scan register on the rising edge of TCK in the Capture-DR controller state.

8.4.3 Boundary Scan register

The function of the assigned bits in this register are described in this section.

This register consists of the following four types of cells:

Table 8.4-2 Cells Types for Pins

Cell Type	Functions
I	This cell type is for all input pins.
O	This cell type is only for the output pins to be set to a logical high or low.
OZ	This cell type is only for DMARQ and INT pins to be set to the logical high, low or the high impedance.
I/O	This cell type is only for data bus pins.

The following pins do not have cell type:

- Digital and Analog Voltage Supplies (VDD, GND, AVDD and AGND)
- Clock Output Pin (XA2)
- Analog Pins (LPF1, LPF2, CGP1 and CGP2)

Because it is meaningless for the voltage supplies to have Boundary Scan registers in order to be able to check these pins by checking whether a instruction can be operated or not.

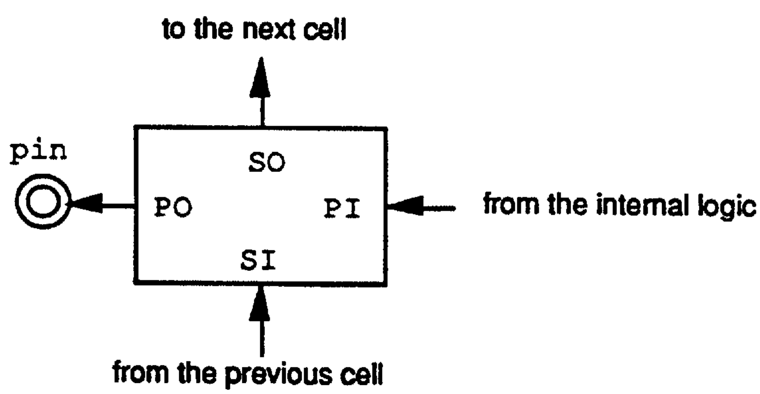
On the other hand, it also is meaningless for the Analog pins to have Boundary Scan registers in order not to be able to output logically.

The Boundary Scan register for the I typed and O typed cells is consisted of the circuitry at the shown in Fig. 8.4.3.1 and Fig 8.4.3.2.

The Boundary Scan register for the I typed cell is consisted of the circuitry at the shown in Fig. 8.4.3.2. As you know from this figure, the input pin is directly connected with the internal logic circuit in the FDC. Because there is some capabilities for the oscillator not to oscillate the self oscillation when the crystal resonator is connected with the XA1 and XA2 pins if some gates are inserted between the pin and the internal logic circuitry in the FDC.

The Boundary Scan register for the OZ typed cells is consisted of the circuitry at the shown in Fig. 8.4.3.3. In this typed cell, the two registers are for the data to be output from the pins and the signal to enable the pins to be output. These OZ typed cells are adapted to the only DMARQ and INT pins.

The Boundary Scan register for the I/O typed cells is consisted of the circuitry at the shown in Fig. 8.4.3.4. In this typed cell, the three registers are for the data to be output from the pins to the internal circuitry in the FDC, the signal to enable the pins to be output and the data to be input from the pins to the internal circuitry in the FDC. These I/O cell types are adapted to the only from DB0 to DB7 pins.



typed O cell for all output pins

Fig 8.4.3.1 the O typed cells

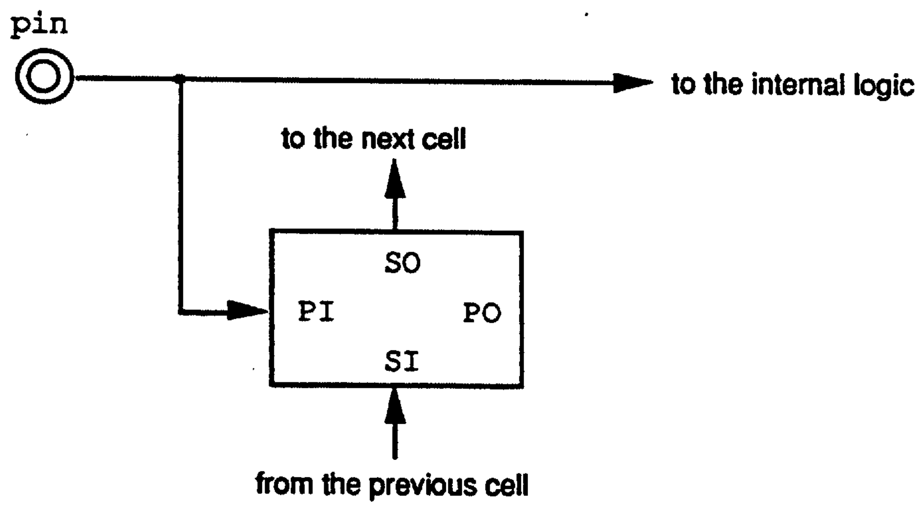


Fig 8.4.3.2 the I typed cell

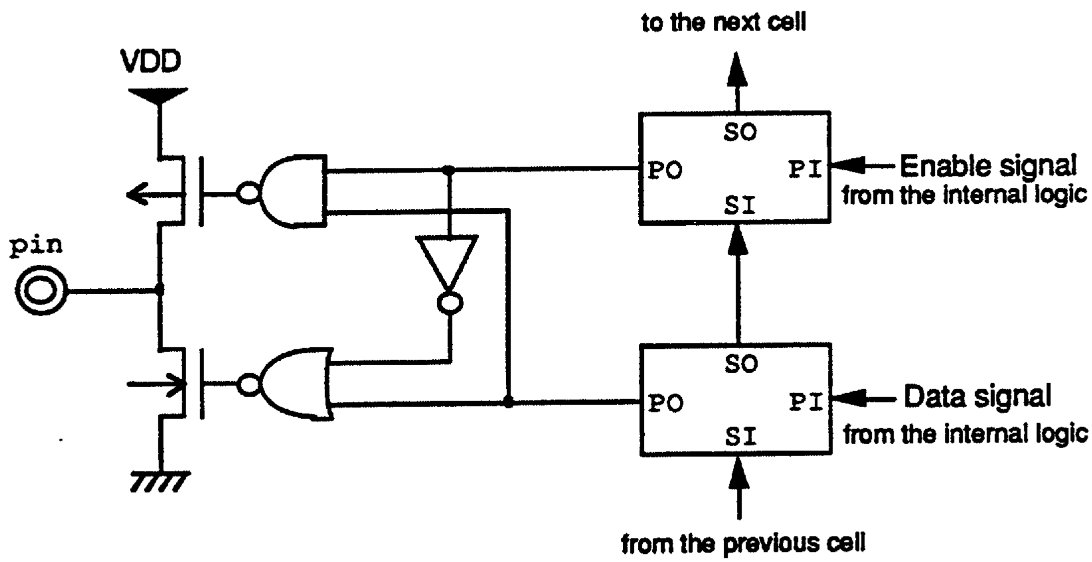


Fig 8.4.3.3 the three states typed cell

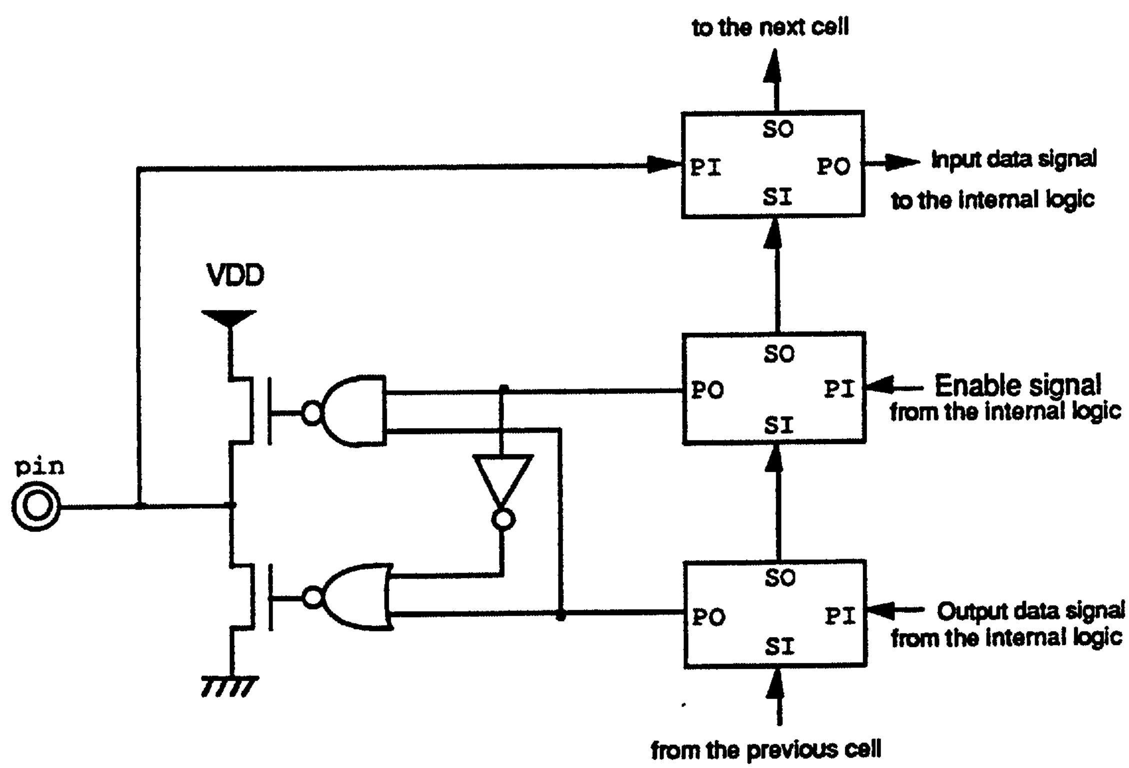


Fig 8.4.3.4 the I/O typed cell

Bit #	Function
D0	Data to be output from the DEN1_B
D1	Data to be output from the DEN0_B
D2	Data to be output from the SEL (HDLD_B)
D3	Data to be output from the DS3_B
D4	Data to be output from the INDEX_B
D5	Data to be output from the DS0_B
D6	Data to be output from the DS1_B
D7	Data to be output from the DS2_B
D8	Data to be output from the ME0_B
D9	Data to be output from the ME1_B
D10	Data to be output from the CA0 (DIR_B)
D11	Data to be output from the CA1 (STEP_B)
D12	Data to be output from the CA2 (SIDE_B)
D13	Data to be output from the LSTRB (NC)
D14	Data to be output from the ENBL0_B (ME2_B)
D15	Data to be output from the ENBL1_B (ME3_B)
D16	Data to be output from the WDATA_B
D17	Data to be output from the WGATE_B
D18	Data to be output from the (TRK0_B)
D19	Data to be output from the (WPRT_B)
D20	Data to be output from the RDATA_B)
D21	Data to be output from the (DKCG_B / READY_B)
D22	Data to be output from the PCTYP1
D23	Data to be output from the PCTYP0
D24	Data to be output from the DRV2
D25	Data to be output from the XB
D26	Data to be output from the XA1
D27	Data to be output from the ENDKCG_B
D28	Data to be output from the TC
D29	Data to be output from the DMARQ

Bit #	Function
D30	Signal to enable the DMARQ active
D31	Data to be output from the INT
D32	Signal to enable the INT active
D33	Data to be input from the DB7
D34	Signal to enable the DB7 active
D35	Data to be output from the DB7
D36	Data to be input from the DB6
D37	Signal to enable the DB6 active
D38	Data to be output from the DB6
D39	Data to be input from the DB5
D40	Signal to enable the DB5 active
D41	Data to be output from the DB5
D42	Data to be input from the DB4
D43	Signal to enable the DB4 active
D44	Data to be output from the DB4
D45	Data to be input from the DB3
D46	Signal to enable the DB3 active
D47	Data to be output from the DB3
D48	Data to be input from the DB2
D49	Signal to enable the DB2 active
D50	Data to be output from the DB2
D51	Data to be input from the DB1
D52	Signal to enable the DB1 active
D53	Data to be output from the DB1
D54	Data to be input from the DB0
D55	Signal to enable the DB0 active
D56	Data to be output from the DB0
D57	Data to be input from the A2
D58	Data to be input from the A1
D59	Data to be input from the A0

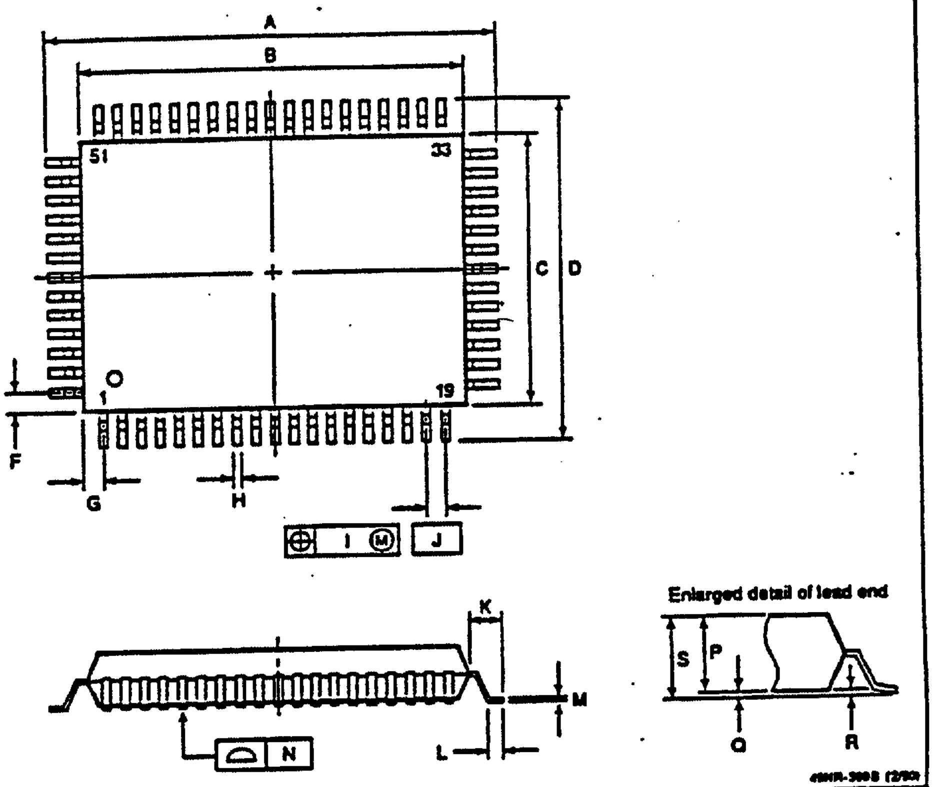
Bit #	Function
D60	Data to be input from the CS_B
D61	Data to be input from the WR_B
D62	Data to be input from the RD_B
D63	Data to be input from the DMAAK_B
D64	Data to be input from the RESET

Appendix

uPD72070 Package Specifications

64-Pin Plastic QFP (2.7 mm thick)

Item	Millimeters	Inches
A	23.6 ±0.4	.929 ±.016
B	20.0 ±0.2	.795 +.009 −.008
C	14.0 ±0.2	.551 +.009 −.008
D	17.6 ±0.4	.693 ±.016
F	1.0	.039
G	1.0	.039
H	0.40 ±0.10	.016 +.004 −.005
I	0.20	.008
J	1.0 (TP)	.039 (TP)
K	1.8 ±0.2	.071 +.008 −.009
L	0.8 ±0.2	.031 +.009 −.008
M	0.15 +0.10 −0.05	.006 +.004 −.003
N	0.15	.006
P	2.7	.106
Q	0.1 ±0.1	.004 ±.004
R	0.1 ±0.1	.004 ±.004
S	3.0 max	.119 max



P64GF-100-388, 3BE-1

3) DUMP AFTER DATA ADDRESS MARK

When the RDM bits are set to "10", this mode can be entered under the only Apple mode.

This dumps the requested number of bytes from the specified track. Especially under the MFM format, after the FDC finds out the specified ID address mark, the Data Address mark of this specified ID field and then the nearest SYNC bytes, the FDC checks whether the next data after these SYNC bytes is equal to the Mark byte, which is expected as the $A1 for Data byte and the $0A for Clock byte. If this mark is hit, the FDC should start to dump data from and including this Mark byte. But if the Mark byte can not be hit, the FDC changes the expected Data for the Mark byte from the above data to the $C2 for Data byte and the $14 for Clock byte and then the FDC resumes to search the same specified ID field.

After the FDC finds out the specified ID address mark and then the nearest SYNC bytes, the FDC checks whether the data after these SYNC bytes is equal to the Mark byte, which is expected as the $C2 for Data byte and the $14 for Clock byte. If this mark is hit, the FDC should start to dump data from and including this Mark byte. But if the mark byte can not be hit, the FDC abnormally terminates the command and interrupts to inform to the host this abnormal termination.

For GCR format, after the FDC finds out the specified ID address mark and then the Data header of this specified ID field, the FDC is waiting to received the Mark byte with the $D5 for Data byte. If this mark is hit, the FDC should immediately start to dump data from and including this Mark byte. But if the mark byte can not be hit, the FDC abnormally terminates the command and interrupts to inform to the host this abnormal termination. In addition, the FDC dumps the data without denibblizing the read-data from the FDD.

The Fig. 4. 18. 3 is shown as a example of this mode. In this example, the ID Address mark is located after the specified ID field, the Data Address mark and the SYNC bytes.

In this dumped mode, the FDC ignores the following errors after the first Address mark in the data field is found out.

- Read error for CRC for the MFM format or Checksum for the GCR format
- Read error for Bit slip byte for the GCR format
- Read error for Address mark in the Data field

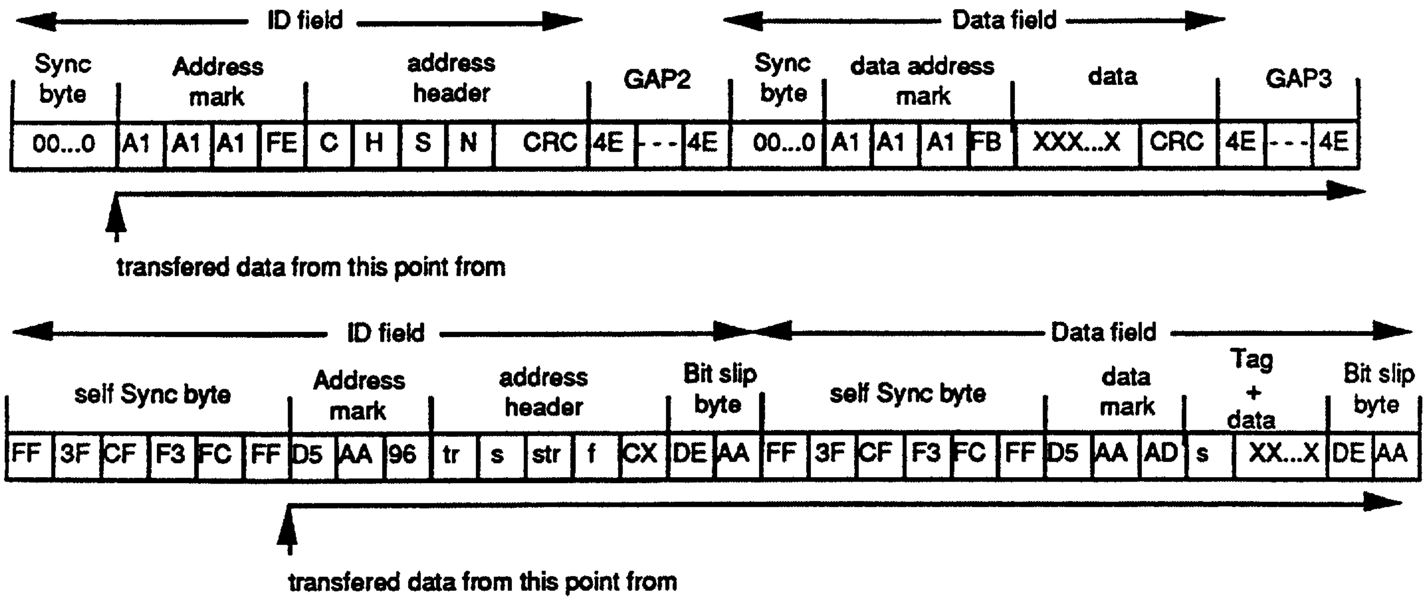


Fig. 4.18.3 Transferred Data for Dump After Data Address Mark

Transferred Data

FOR MFM FORMAT

The FDC starts to dump data to the host according to the following transfer rule shown in the Fig. 4.18.4 after the mark byte is detected. This transfer is called the 8 x 8 data transfer format and the FDC should transfer the Data byte and the Clock byte, repeatedly.

Data from the FDD

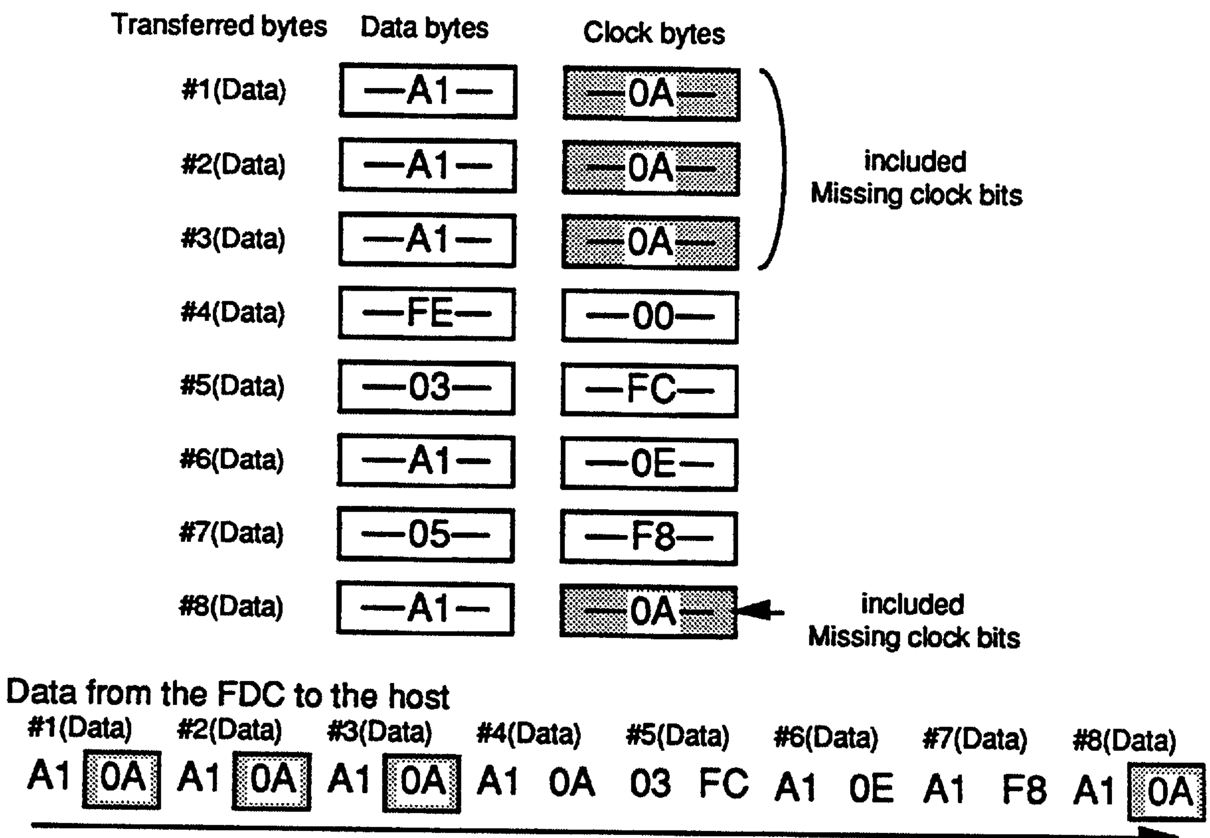


Fig. 4.18.4 The 8 X 8 Data Transfer Format for MFM

The following charts illustrate the MFM clock byte for the dumped data pattern. The chart shows two clock bytes for each data pattern. The clock0 column illustrates the clock byte if the previous data bit was a "0". The clock1 column illustrates the clock byte if the previous data bit was a "1".

data	clock0	clock1	data	clock0	clock1	data	clock0	clock1	data	clock0	clock1
00	ff	fe	20	f3	f2	40	f9	f8	60	f1	f0
01	7f	7e	21	73	72	41	79	78	61	71	70
02	3f	3e	22	33	32	42	39	38	62	31	30
03	3f	3e	23	33	32	43	39	38	63	31	30
04	9f	9e	24	93	92	44	99	98	64	91	90
05	1f	1e	25	13	12	45	19	18	65	11	10
06	1f	1e	26	13	12	46	19	18	66	11	10
07	1f	1e	27	13	12	47	19	18	67	11	10
08	cf	ce	28	c3	c2	48	c9	c8	68	c1	c0
09	4f	4e	29	43	42	49	49	48	69	41	40
0a	0f	0e	2a	03	02	4a	09	08	6a	01	00
0b	0f	0e	2b	03	02	4b	09	08	6b	01	00
0c	8f	8e	2c	83	82	4c	89	88	6c	81	80
0d	0f	0e	2d	03	02	4d	09	08	6d	01	00
0e	0f	0e	2e	03	02	4e	09	08	6e	01	00
0f	0f	0e	2f	03	02	4f	09	08	6f	01	00
10	e7	e6	30	e3	e2	50	e1	e0	70	e1	e0
11	67	66	31	63	62	51	61	60	71	61	60
12	27	26	32	23	22	52	21	20	72	21	20
13	27	26	33	23	22	53	21	20	73	21	20
14	87	86	34	83	82	54	81	80	74	81	80
15	07	06	35	03	02	55	01	00	75	01	00
16	07	06	36	03	02	56	01	00	76	01	00
17	07	06	37	03	02	57	01	00	77	01	00
18	c7	c6	38	c3	c2	58	c1	c0	78	c1	c0
19	47	46	39	43	42	59	41	40	79	41	40
1a	07	06	3a	03	02	5a	01	00	7a	01	00
1b	07	06	3b	03	02	5b	01	00	7b	01	00
1c	87	86	3c	83	82	5c	81	80	7c	81	80
1d	07	06	3d	03	02	5d	01	00	7d	01	00
1e	07	06	3e	03	02	5e	01	00	7e	01	00
1f	07	06	3f	03	02	5f	01	00	7f	01	00

data	clock0	clock1	data	clock0	clock1	data	clock0	clock1	data	clock0	clock1
80	fc	fc	a0	f0	f0	c0	f8	f8	e0	f0	f0
81	7c	7c	a1	70	70	c1	78	78	e1	70	70
82	3c	3c	a2	30	30	c2	38	38	e2	30	30
83	3c	3c	a3	30	30	c3	38	38	e3	30	30
84	9c	9c	a4	90	90	c4	98	98	e4	90	90
85	1c	1c	a5	10	10	c5	18	18	e5	10	10
86	1c	1c	a6	10	10	c6	18	18	e6	10	10
87	1c	1c	a7	10	10	c7	18	18	e7	10	10
88	cc	cc	a8	c0	c0	c8	c8	c8	e8	c0	c0
89	4c	4c	a9	40	40	c9	48	48	e9	40	40
8a	0c	0c	aa	00	00	ca	08	08	ea	00	00
8b	0c	0c	ab	00	00	cb	08	08	eb	00	00
8c	8c	8c	ac	80	80	cc	88	88	ec	80	80
8d	0c	0c	ad	00	00	cd	08	08	ed	00	00
8e	0c	0c	ae	00	00	ce	08	08	ee	00	00
8f	0c	0c	af	00	00	cf	08	08	ef	00	00
90	e4	e4	b0	e0	e0	d0	e0	e0	f0	e0	e0
91	64	64	b1	60	60	d1	60	60	f1	60	60
92	24	24	b2	20	20	d2	20	20	f2	20	20
93	24	24	b3	20	20	d3	20	20	f3	20	20
94	84	84	b4	80	80	d4	80	80	f4	80	80
95	04	04	b5	00	00	d5	00	00	f5	00	00
96	04	04	b6	00	00	d6	00	00	f6	00	00
97	04	04	b7	00	00	d7	00	00	f7	00	00
98	c4	c4	b8	c0	c0	d8	c0	c0	f8	c0	c0
99	44	44	b9	40	40	d9	40	40	f9	40	40
9a	04	04	ba	00	00	da	00	00	fa	00	00
9b	04	04	bb	00	00	db	00	00	fb	00	00
9c	84	84	bc	80	80	dc	80	80	fc	80	80
9d	04	04	bd	00	00	dd	00	00	fd	00	00
9e	04	04	be	00	00	de	00	00	fe	00	00
9f	04	04	bf	00	00	df	00	00	ff	00	00

FOR GCR FORMAT

The FDC starts to dump the raw data from FDD to the host without denibblizing, this **disables** the 3 - 4 conversion process. In addition, the data that is transferred from the FDC to the host is in the 8x8 format. The difference is that the clock byte that is transferred is a duplicate of the data byte. This additional Dummy Clock byte is meaningless. Please refer to the following diagram.

Data from the FDD

Transferred bytes	Data bytes	Dummy Clock bytes
#1(Data)	—FA—	—FA—
#2(Data)	—9D—	—9D—
#3(Data)	—A7—	—A7—
#4(Data)	—FE—	—FE—
#5(Data)	—FB—	—FB—
#6(Data)	—AB—	—AB—
#7(Data)	—BA—	—BA—
#8(Data)	—DD—	—DD—

Data from the FDC to the host

#1(Data)	#2(Data)	#3(Data)	#4(Data)	#5(Data)	#6(Data)	#7(Data)	#8(Data)
FA FA	9D 9D	A7 A7	FE FE	FB FB	AB AB	BA BA	DD DD

Fig. 4.18.5 The 8 X 8 Data Transfer Format for GCR

ERROR CONDITIONS

1) DUMP AFTER THE ID ADDRESS MARK:

If the recording format is GCR and the FDC can not find the ID Address Mark within the 400msec.

If the recording format is MFM and the FDC can not find the ID Address Mark within two Index pulses.

2) DUMP AFTER THE DATA ADDRESS MARK:

If the recording format is GCR and the FDC can not find a Data Address Mark within the 400msec.

If the recording format is MFM and the FDC can not find the Data Address Mark within two Index pulses.

3) WHEN THE FOLLOWING CONDITIONS OCCUR:

- The overrun or underrun occur during the data transfer.
- The TC does not be input for the allowable period.
- Under Standard modes, the READY_B pin in the drive interface is inactive before this is operated under Standard modes.

Under Standard modes:

This command is similar to the above function under the Apple mode, except that this is a continuous read operation from the data field of the sectors immediately after the Index pulse.

PARAMETERS IN THE RESULTANT PHASE

*1) # OF SECTOR TO BE READ

For Apple mode, this byte indicates the number of remaining sectors to be read when this command has failed by some error.

# of Sector to be Read" (Resultant Phase) = # of Sectors to be Read - # of Sector Read"

For example, the host has set 5 to the byte "# of Sectors to be Read" in the Command Phase. When the FDC detects some error while it is reading the third sector to be read (after the first and second sectors were successfully read), the FDC reports in the resultant phase that this "# of Sector to be read" byte is set "3" (5-2).

The parameters in this command are same functions as the Read Data Commands except the parameters specified above.

ERROR CONDITIONS

1) When the FDC can not find the following within 400msec for the GCR format, or when the FDC can not find the following before two Index pulses are detected for MFM and FM format:

- Address mark in the Address header (ID field)
- Desired Address header (Data in the ID field)

2) When the FDC detects a Read Error in the following:

- CRC bytes or the Checksum bytes
- Address Mark in the Data field
- Bits slip bytes (Under GCR format only)

3) When the following conditions occur:

- Overrun or Underrun occur during Data transfer.
- When utilizing the TC input, it does not meet the correct

timing period.

- Under Standard/Apple mode, when the status of the FDD indicates a NOT READY condition prior to command execution.
- Under Standard modes, when the DDAM (Deleted Data Address Mark) is detected, the CM bit of the Status Register 2 (ST2) is set. and one of the following two conditions occur according to the contents of the TB bit in the command phase.

  (1) When TB=0: command execution terminates normally after data transfer of that sector. The ID bytes of the sector in which DDAM is detected will be the value in the result phase.

  (2) When TB=1: the sector is skipped and the next sector is read.

4) When the FDC continues to read even if the following errors occur:

- The CRC bytes or the Checksum bytes
- The Bits slip bytes (only under GCR format) but the FDC will mark the error in the Status register 0-2 at the result phase.

Phase	R/W	D7 D6 D5 D4 D3 D2 D1 D0	Remarks
command	W	MT FM TB 0 0 1 1 0	command code
	W	X X X X X HD DR1 DR0	
	W	Cylinder	
	W	Head	
	W	Sector	
	W	(Bytes/Sector) / Format Byte	
	W	Last Sector in Muliti Sector Read	
	W	GSL(MFM) / don't care (GCR)	
	W	Data Length in Bytes	
Execution			data transfer between Host and FDD
	R	Status Regisiter 0	status information after this command
	R	Status Regisiter 1	
	R	Status Regisiter 2	
	R	Cylinder	
	R	Head	
	R	Sector	
	R	(Bytes/Sector) / Format Byte	

FUNCTION

GENERAL: The host can use this command to read the data in the Data field from the specified sector. After this command has been issued, the FDC begins reading ID address header (or data in the ID field).

When the specified sector number equals the sector number read off the disk, the FDC transfers the data from the Data field byte by byte via the data bus.

After completion of this operation from the current sector, the internal sector number is incremental by one, and the data from the next sector is read and output on the data bus.

MULTI-TRACK READ: If the MT (Multi-track) bit is set, the read will continue with data on the other side of the disk, for the specified cylinder only.

TAG BYTE FOR THE ONLY GCR FORMAT:

While in the GCR format, the FDC will ignore the Tag bytes at the

beginning of the sector, unless the TB bit is set to high(1). When the TB bit is set to high(1), the FDC will transfer 524 bytes to the host. If the TB bit is not set, the FDC will transfer only the 512 data bytes of the sector.

PARAMETERS

a.) GCR format:

The values for the EOT (Last Sector in the Multi-sector Read) and N (bytes/sector) should be set as:

N should be set as 02H, 22H, or 24H

EOT should be set from 8H to CH

b.) MFM or FM format:

The reference value for the EOT, N, and GSL are shown in Table 4.8.1

Format	Bytes/sector	N(16)	EOT(16)	GSL(16)	Notes
MFM	256	01	1A	0E	IBM diskette 2D
	512	02	09	1B	720KB
	512	02	0F	1B	1.2MB
	512	02	12	1B	1.44MB
	512	02	24	1B	2.88MB
	1024	03	08	35	IBM diskette 2D
	2048	04	04	Undetermined	
	4096	05	02	Undetermined	
	8192	06	01	Undetermined	
FM	128	00	1A	07	IBM diskette 1
	256	01	0F	0E	IBM diskette 2
	512	02	08	1B	
	1024	03	04	Undetermined	
	2048	04	02	Undetermined	
	4096	05	01	Undetermined	

Table 4.8.1 Reference Values for N and EOT

DATA LENGTH IN A SECTOR:

For Standard modes, only when the "Number of data bytes in the Sector" byte (N) is Zero for the FM format, this data length in the sector is determined by the "Data length in bytes" byte (DTL). This "DTL" should be set the less than 80H and 128bytes/sector is specified when this "DTL" is set the bigger than 80H.

When the "Number of data bytes in the Sector" byte (N) is not zero, this data length is determined by the only "Number of data bytes in the Sector" byte (N) (see the above table 4.8.1).

NORMAL TERMINATION

When this command normally terminates, the values in Table 4.8.1 are set at the resultant phase:

MT	Head	last sector	ID information at the result phase			
			Cylinder	Head	Sector	N
0	0	< EOT	NC	NC	S+1	NC
0	0	= EOT	C+1	NC	1	NC
0	1	< EOT	NC	NC	S+1	NC
0	1	= EOT	C+1	NC	1	NC
1	0	< EOT	NC	NC	S+1	NC
1	0	= EOT	NC	1	1	NC
1	1	< EOT	NC	NC	S+1	NC
1	1	= EOT	C+1	0	1	NC

Table 4.8.1 Normally Terminated Values for Read Data Command

NC — No Change

EOT — Maximum number of sectors to be written on the disk

LAST SECTOR — Number of the "last sector in the Multi sector read" byte at the command phase

C — Number of the "Cylinder" bytes at the command phase

S — Number of the "Sector" bytes at the command phase

N — "Number of data bytes written" at the command phase

PARAMETERS

FM — Under Apple mode, this bit indicates the following format mode:

MFM format mode, when this bit is set.

GCR format mode, when this bit is reset.

Under Standard modes, this bit indicates the following format mode:

MFM format mode (when this bit is set).

FM format mode (when this bit is reset).

TB — Under Apple mode, this bit determines whether the data in Tag bytes should be transferred or not.

Transfers the data (when this bit is set).

Don't transfer the data (when this bit is reset.

Under Standard modes, this bit determines whether the data in the Data field are skipped or not.

Skips the data	(when this bit is set).
Transfers the data	(when this bit is reset).

MT Under Standard modes, the issued command requests the FDC to perform the Seek command without specially issuing the Seek command and then to perform this Read Data command, when this bit is set.

ERROR CONDITIONS

1) When the FDC can not find the following within the 400msec. in Apple mode or when the FDC can not find the following before two Index pulses are input for MFM and FM format in standard mode:

- Address mark in the Address header (ID field)
- Desired Address header (data in the ID field)

2) When the FDC detects a read error in the following:

- the CRC bytes or the Checksum bytes
- the address mark in the Data field
- the Bits slip bytes under only GCR format

3) When the following conditions occur:

- The overrun or underrun occur during the data transfer.
- When utilizing the TC input, it does not meet the correct timing period.
- Under Standard modes, the READY_B pin in the drive interface is inactive before this is operated under Standard modes.
- Under Standard modes, when the DDAM (Deleted Data Address Mark) is detected, the CM bit of the Status Register 2 (ST2) is set and one of the following two conditions occur according to the contents of the TB bit in the command phase.

  (1) When TB=0: Command execution terminates normally after data transfer of that sector. The ID bytes of the sector in which DDAM is detected will be the value in the result phase.

  (2) When TB=1: The sector is skipped and the next sector is read.

Phase	R/W	D7 D6 D5 D4 D3 D2 D1 D0	Remarks
command	W	MT FM SK 0 1 1 0 0	command code
	W	X X X X X HD DR1 DR0	
	W	Cylinder	
	W	Head	
	W	Sector	
	W	Number of data bytes in the Sector	
	W	Last Sector in Muliti Sector Read	
	W	GSL	
	W	Data Length in Bytes	
Execution			data transfer between Host and FDD
Result	R	Status Regisiter 0	status information after this command
	R	Status Regisiter 1	
	R	Status Regisiter 2	
	R	Cylinder	
	R	Head	
	R	Sector	
	R	Number of data bytes read	

FUNCTION

This command can be used only under Standard modes and can not be supported under Apple mode.

DAM and DDAM explained in the Read Data functions under standard modes are replaced with DDAM and DAM, respectively.

Read ID

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
command	W	0	FM	0	0	1	0	1	0	command code
	W	X	X	X	X	X	HD	DR1	DR0	
Execution										The first correct ID information found on the track is returned
	R	Status Regisiter 0								status information after this command
	R	Status Regisiter 1								
	R	Status Regisiter 2								
	R	Cylinder								
	R	Head								
	R	Sector								
	R	(Bytes/Sector) / Format Byte								

FUNCTION

The host uses this command to read the present position of the Read/Write head of the FDD. The FDC returns the first available address header (or data in the ID field), after a sync byte field, during the result phase.

ERROR CONDITIONS

FOR MFM FORMAT:

If the FDC can not find the requested data in the ID field before two Index pulses have passed, the FDC will terminate this command and inform the host via the status passed in the result phase.

FOR GCR FORMAT:

If the FDC can not find the requested address header before two revolutions have occurred within 400msec, the FDC will terminate this command and inform the host via the status passed in the result phase.

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	0	0	0	0	1	1	1	command code
	W	X	X	X	X	X	X	DR1	DR0	
Execution										Head is recalibrated cylinder 0.

FUNCTION

This command causes the FDD to retract the Read/Write head to Cylinder 0.

Under Apple mode: After the FDC receives this command and resets the internal parameter of PCN byte:

(1) The FDC first issues the /Step command toward the outside to the FDD for 80 steps and then checks the status of /Track0 from the FDD.

(2) After the status of /Track0 becomes active, the FDC issues the /Step command toward the inside to the FDD until the status of /Track0 becomes inactive.

(3) After the status of /Track0 becomes inactive and then the FDC issues a /Step command toward the outside to the FDD, the FDC confirms the active status of /Track0.

(4) The interrupt (INT) is asserted to inform of the host about the termination of this command.

(5) Finally, the result for this command is reflected in the Status Register 0 (ST0) and this ST0 should be read by issuing the Sense Interrupt Status command.

Under Standard modes: After the FDC resets the internal parameter of PCN byte, a Seek Operation is performed toward the outside until TRK0_B signal in the drive interface becomes active.

When the TRK0_B signal becomes active, the SE bit in the Status Register 0 is set and the command execution is normally terminated. However, this Status Register 0 should need to be read by issued the Sense Interrupt Status command.

ERROR CONDITIONS

UNDER APPLE MODE:

The FDC informs the host of a abnormal terminations by setting the INT pin active after the EC bit in the Status register 0 in the result phase is set.

(1) The FDC first issues the /Step command toward the outside to the FDD

for a maximum of 80 steps, the FDC can not check the active status of /Ready in the drive interface within 800msec after the last /STEP command is issued.

(2) After the FDC checks the active status of /Ready in the drive interface within 800msec after the last /STEP, the FDC can not check the active status of /Track0 in the drive interface.

(3) After the status of /Track0 becomes active and the FDC issues the /Step command toward the inside to the FDD for a maximum of 80 steps, the FDC can not check the inactive status of /Track0.

(4) After the FDC issues a /Step command to the FDD in the above sequence, the FDC can not check the active status of /Ready in the drive interface within 18msec.

(5) After the status of /Track0 becomes inactive and then the FDC issues a /Step command toward the outside to the FDD, the FDC can not confirms the active status of /Track0.

(6) After the FDC issues a /Step command to the FDD in the above sequence, the FDC can not check the active status of /Ready in the drive interface within 18msec..

UNDER STANDARD MODE:

(1) When the TRK0_B signal does not become active after issuing the maximum of 80 steps to FDD, the FDC sets the SE and EC bits in the Status register 0.

(2) When the READY_B signal becomes inactive during the execution phase, the FDC sets the SE and NR bits in the Status register 0.

Relative Seek

Phase	R/W	D7 D6 D5 D4 D3 D2 D1 D0	Remarks
command	W	1 DIR 0 0 1 1 1 1	command code
	W	X X X X X HD DR1 DR0	
	W	Relative cylinderNumber	
Execution			Head is positioned over relative cylinder.

FUNCTION

This command is used under Standard modes. The FDC relatively seeks the Read/Write head to the destination cylinder according to the number of the "Relative cylinder Number" byte. The direction is defined by the DIR bit.

Revision

Phase	R/W	D7 D6 D5 D4 D3 D2 D1 D0	Remarks
command	W	0 0 1 0 0 0 0 0	command code
Result	R	D7 D6 D5 D4 D3 D2 D1 D0	Echo back the revision of installed Firmware.
Result	R	D7 D6 D5 D4 D3 D2 D1 D0	Echo back the revision of installed Hardware.

FUNCTION

Under all modes, the result of this command indicates the revision number of both the firmware and hardware installed into this FDC. The number starts from the zero to "FF".

The Operating System can easily know what number the installed firmware is running in the FDC.

ERROR CONDITIONS

There are no error conditions for this command.

Scan Equal

Phase	R/W	D7 D6 D5 D4 D3 D2 D1 D0	Remarks
command	W	MT FM SK 1 0 0 0 1	command code
	W	X X X X X HD DR1 DR0	
	W	Cylinder	
	W	Head	
	W	Sector	
	W	Number of data bytes in the Sector	
	W	Last Sector in Muliti Sector Read	
	W	GSL	
	W	STP	
Execution			data transfer between Host and FDD
Result	R	Status Regisiter 0	status information after this command
	R	Status Regisiter 1	
	R	Status Regisiter 2	
	R	Cylinder	
	R	Head	
	R	Sector	
	R	Number of data bytes read	

FUNCTION

This command is used under Standard modes. This has the same function as the Read Data command.

Data Comparison

When a data byte transferred from the host is set to FFH, the FDC does not compare with a data from the FDD. (It is assumed to be equal.)

Comparison Method

A check is made to see if the data byte string on the sector to be compared is equal to the system data string. If equal, command execution terminates normally.

		MSB
DISK	Data Address Mark	01 02 03 FF 05 06 -------- FE
HOST		01 02 03 FF 05 06 -------- FE
		l–> Disk=host (not compared)

Fig. 4.22.1

SECTOR UPDATE

When a data string on one sector is compared with the host data string and the comparison condition is not satisfied, the internal sector number (S) to be found out is updated (S <--- S + STP, where STP should be 1 or 2), and the data string on the sector specified in the sector number is compared with the host data string. Therefore, the host should send the same data string repeatedly for each sector.

STP

The STP parameter should be set to 01H or 02H. When it is set to 02H, the sector number (S) and the Last Sector in Multi Sector Read (EOT) must be set so as to satisfy the following expression:

$$S + 2(n-1) = EOT$$

Where n is the number of sectors to be read.

EXECUTION TERMINATION

When a comparison is made on a sector and if the sector satisfies the comparison condition, then command execution terminates normally. If the equal condition is satisfied, SH bit in the Status register 2 (ST2) is set. When there are no sectors satisfying the comparison condition although a comparison is made from the first to last sector, the SN bit in the Status register is set and command execution terminates normally.

Scan High or Equal

Phase	R/W	D7 D6 D5 D4 D3 D2 D1 D0	Remarks
command	W	MT FM SK 1 1 1 0 1	command code
	W	X X X X X HD DR1 DR0	
	W	Cylinder	
	W	Head	
	W	Sector	
	W	Number of data bytes in the Sector	
	W	Last Sector in Muliti Sector Read	
	W	GSL	
	W	STP	
Execution			data transfer between Host and FDD
Result	R	Status Regisiter 0	status information after this command
	R	Status Regisiter 1	
	R	Status Regisiter 2	
	R	Cylinder	
	R	Head	
	R	Sector	
	R	Number of data bytes read	

FUNCTION

This command is used under Standard modes. This command has the same function as the Read Data command.

Data comparison

When a data byte transferred from the host is set to FFH, the FDC does not compare with a data from the FDD. (It is assumed to be equal.)

Comparison method

When the data byte string on the sector to be compared is greater than or equal to the host data string, command execution terminates normally.

		MSB							
DISK	Data Address Mark	01	02	03	44	05	06	--------	FE
HOST		01	02	03	40	05	06	--------	FE

|--> Disk>host (compared)

Fig. 4.24.1

SECTOR UPDATE

When a data string on one sector is compared with the host data string and the comparison condition is not satisfied, the internal sector number (S) to be found out is updated (S <--- S + STP, where STP should be 1 or 2), and the data string on the sector specified in the sector number is compared with the host data string.

Therefore, the host should send the same data string repeatedly for each sector.

STP

The STP parameter should be set to 01H or 02H. When it is set to 02H, the sector number (S) and the Last Sector in Multi Sector Read (EOT) must be set so as to satisfy the following expression:

$$S + 2(n - 1) = EOT$$

Where n is the number of sectors to be read.

EXECUTION TERMINATION

When a comparison is made on a sector and if the sector satisfies the comparison condition, then command execution terminates normally. If the equal condition is satisfied, SH bit in the Status register 2 (ST2) is set. When there are no sectors satisfying the comparison condition although a comparison is made from the first to last sector, the SN bit in the Status register is set and command execution terminates normally.

Scan Low or Equal

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
command	W	MT	FM	SK	1	1	0	0	1	command code
	W	X	X	X	X	X	HD	DR1	DR0	
	W	Cylinder								
	W	Head								
	W	Sector								
	W	Number of data bytes in the Sector								
	W	Last Sector in Muliti Sector Read								
	W	GSL								
	W	STP								
Execution										data transfer between Host and FDD
Result	R	Status Regisiter 0								status information after this command
	R	Status Regisiter 1								
	R	Status Regisiter 2								
	R	Cylinder								
	R	Head								
	R	Sector								
	R	Number of data bytes read								

FUNCTION

This command is used under Standard modes. This command has the same function as the Read Data command.

Data Comparison

When a data byte transferred from the host is set to FFH, the FDC does not compare with a data from the FDD. (It is assumed to be equal.)

Comparison Method

When the data byte string on the sector to be compared is less than or equal to the host data string, command execution terminates normally.

MSB

DISK Data Address Mark 01 02 03 04 05 06 -------- FE

HOST 01 02 03 40 05 06 -------- FE

1–> Disk<host (compared)

Fig. 4.23.1

SECTOR UPDATE

When a data string on one sector is compared with the host data string and the comparison condition is not satisfied, the internal sector number (S) to be found out is updated (S <--- S + STP, where STP should be 1 or 2), and the data string on the sector specified in the sector number is compared with the host data string. Therefore, the host should send the same data string repeatedly for each sector.

STP

The STP parameter should be set to 01H or 02H. When it is set to 02H, the sector number (S) and the Last Sector in Multi Sector Read (EOT) must be set so as to satisfy the following expression:

$$S + 2(n - 1) = EOT$$

Where n is the number of sectors to be read.

EXECUTION TERMINATION

When a comparison is made on a sector and if the sector satisfies the comparison condition, then command execution terminates normally. If the equal condition is satisfied, SH bit in the Status register 2 (ST2) is set. When there are no sectors satisfying the comparison condition although a comparison is made from the first to last sector, the SN bit in the Status register is set and command execution terminates normally.

inform this termination of the host. This status register 0 should be read by issued the Sense Interrupt Status command.

Since the FDC is not busy in the Execution phase, seek or recalibrate commands given to other FDDs are accepted and seek operation can be performed on up to four FDD at the same time. But Read/Write groups commands must not be issued during the seek operation.

ERROR CONDITIONS

UNDER APPLE MODE

If the /Ready line does not become active following a /Step command, within the allowable time specified in following table 4.4.1, the FDC will terminate this command. Upon termination, the FDC will assert an interrupt, set the EC bit in the status register 0 and indicate an abnormal termination. The maximum timeout for all possible condition is 800msec.

Max Waiting Time	Conditions
18msec	When the Seek operation to move one track without speed block change under GCR and MFM
250msec	When the Seek operation to move one track with speed block change (only GCR mode)
800msec	When the Seek operation to move tracks with more than two speed block changes under both GCR and MFM

Table 4.4.1 Allowable Waiting Time for /Ready Status after /Step Command is Issued

UNDER STANDARD MODES:

When the READY_B signal becomes inactive during the execution phase, the FDC sets the SE and NR bits in the Status register 0.

Sense Drive Status

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
command	W	0	0	0	0	0	1	0	0	command code
	W	X	X	X	X	X	HD	DR1	DR0	
Result	R	Status Register 3								Status information for FDD

FUNCTION

This command reports the status of the FDD by reading the Status Register 3 (ST3) from the Data register.

PARAMETERS IN THE RESULTANT PHASE

Under Apple mode:

The Status Register 3 (ST3) is shown in the following diagram:

D7	D6	D5	D4	D3	D2	D1	D0
Media	WP	RY	T0	DRIVE	MODE	SEL MEDIA	MFM

Status Register 3 (ST3) under Apple Mode

MEDIA	Reflects the /2MB or /4MB media status from FDD
WP	Reflects the /WRTPRT status from FDD
RY	Reflects the /READY status from FDD
T0	Reflects the /TK0 status from FDD
DRIVE	Reflects the 2MB-4MB Drive status from FDD
MODE	Reflects the /Mode ID status from FDD
SEL MEDIA	Reflects the /Select Media status from FDD
MFMM	Reflects the /MFM mode status from FDD

Under Standard Modes:

The Status Register 3 (ST3) is shown in the following diagram:

D7	D6	D5	D4	D3	D2	D1	D0
0	WP	RY	T0	1	HD	DR1	DR0

Status Register 3 (ST3) under Standard Modes

WP	Reflects the state of the WPRT_B pin in the drive interface
RY	Reflects the state of the READY_B pin in the drive interface
T0	Reflects the state of the TRK0_B pin in the drive interface
HD	Reflects the
DR1, DR0	Reflects the

ERROR CONDITIONS

There are no error conditions for this command under both Apple and Standard modes.

Note: Under Apple mode only, this command should be issued to get the correct status from the FDD only after the "Set Enable Control" command is issued. In the other word, if this command is issued to the FDC more than one time after the "Set Enable Control" command is issued, the FDC can not correctly inform to the host the content of the Status register 3 (ST3) at the result phase. Because the specific FDD of Apple has the same codes between the Motor off and the Select Media command to the FDD.

Sense Interrupt Status

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
command	W	0	0	0	0	1	0	0	0	command code
Result	R	Status Register 0								Status for Interrupt
	R	Present CylinderNumber								

FUNCTION

By using this command, the host can check why the FDC has interrupted the host. The interrupts between Apple and Standard operation modes occur for different reasons.

Under Apple mode:

(1) Upon entering the result phase of any commands that passes back some status information.

(2) End of Seek and Recalibrate commands.

(3) End of the following commands:

- Disable/Enable DPLL
- Set Motor Control
- Set Drive Mode
- EJECT Command

The host should issue this command to the FDC within 100ms after the above interrupt occurs. Unless this command can not be issued within this 100ms, these maybe be some capability to miss the already occurred interrupt.

(4) During the execution phase in the non-DMA transfer mode to request more data

(5) /CSTIN status bit from the FDD changes status.

(6) The FDC interrupts when the FDC detects the issued command was invalid. In this case, the host should read the only Status register 0 from the FDC because the FDC can not set the "Present Cylinder Number" (PCN) byte.

Under standard modes:

(1) Upon entering the result phase of any commands that passes back some status information.

(2) The status of READY_B signal in the drive interface is changed for the target of the standard FDDs.

(3) End of Seek and Recalibrate commands

(4) During the execution phase in the non-DMA transfer mode to request more data

(5) The FDC interrupts when the FDC detects the issued command was invalid. In this case, the host should read the only Status register 0 from the FDC because the FDC can not set the "Present cylinder Number" byte.

Talking about the result parameters, this command has two types of result parameters after the FDC suddenly interrupts to the host and then the host issues this command to the FDC.

- One Byte Parameters
- Two Byte Parameters

One Byte Parameters

Regarding one byte parameter in the result parameter, this case occurs after the following:

- The FDC interrupts to the host to inform to detect the status of the target FDD in the polling routine to be waiting for the issued command. Especially, this status means the /CSTIN status from the FDD during the Apple operation mode and the READY_B pin during other operation modes.
- The host issues the Sense Interrupt Status command to the FDC after the interrupts for the following command occur.

- Disable/Enable DPLL	- Set Drive Mode
- Set Motor Control	- EJECT Command

- The host issues the Sense Interrupt Status command to the FDC in spite of not interrupted by the FDC.

Two Byte Parameters

Regarding two byte parameters in the result parameter, this case occurs after the following:

- The FDC interrupts to the host to inform to detect the termination of the Seek or Recalibrate command.

How to Receive Parameter in the Result Phase

The host should know how may bytes should be received from the FDC at the result phase of the Sense Interrupt Status command by checking the first byte at this result parameter. If this first byte indicates either the changed status for the target FDD or the invalid command received from

the host, the host should read only one byte from the FDC at this result phase.

On the other hand, if this first byte indicates the termination of either the Seek or Recalibrate command, the host should read only two byte from the FDC at this result phase.

ERROR CONDITIONS

There are no error conditions for this command under both Apple and Standard modes.

Set Enable Control

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
command	W	EN	0	0	1	1	0	1	1	command code
	W	X	X	X	X	X	X	X	DR	
Execution										Sets or resets Enable Pin according to specified value.

FUNCTION

Under Apple mode only, this command is used to turn on or off the Enable Pin of the specified drive. Once the ENBL_B pin is set active by this command, the ENBL_B pin keeps the same state until this command makes this ENBL_B pin inactive. Only after this command is issued to reset the ENBL_B pin to inactive while this pin is active, this pin is then reset to inactive.

On the other hand, Immediately after asserting or deasserting the ENBL_B Pin of the specified FDD, the FDC will issue a normal termination interrupt to the host.

Note that the ENBL_B Pins of two FDD's can not be set to active at the same time by using this command. In addition, the host should remember which ENBL_B Pin is active because the FDC does not save the status for which FDD is enabled.

Regarding the polling sequence, the FDC can not poll the status for the two FDD's while one ENBL_B Pin is active after this command is issued. This means that the FDC can not detect the event that the media is inserted into another FDD while the ENBL_B Pin is active on another drive. After the ENBL_B Pin is reset to inactive by issuing this command, the FDC can then detect that the media is inserted into another FDD.

PARAMETERS

EN = 1	The ENBL_B Pin of the FDD specified by the DR bit in the second byte is set to the active state.
EN = 0	The ENBL_B Pin of the FDD specified by the DR bit in the second byte is reset to the inactive state.

ERROR CONDITIONS

This command checks no status of the specified FDD therefore this command has no error conditions and the FDC always informs the host of a normal termination.

Set Drive Mode

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
command	W	0	FM	0	1	1	1	0	0	command code
	W	X	X	X	X	X	X	X	DR	
Execution										Sets drive mode to GCR or MFM via the /MFM command according to specified value.

FUNCTION

Under Apple mode only, this command is used to set the drive to either GCR or MFM mode. This is done by writing the /MFM mode control bit in the specified drive. After the /MFM command has been sent to the FDD, the FDC will monitor the /Ready status line to determine whether this command was completed or not. At the completion of the command, the FDC will issue a normal termination interrupt.

ERROR CONDITIONS

If the /Ready line is not asserted within 800msec after the command is asserted, the FDC should abort the command and issue an interrupt. When the interrupt is asserted, the FDC should mark the command as abnormally terminated and assert the EC bit in the Status register 0 (ST0). The host will then issue a Sense Interrupt Status command to be read the EC bit.

Set Motor Control

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
command	W	MO	0	0	1	1	0	1	0	command code
	W	X	X	X	X	X	X	X	DR	
Execution										Sets /MOTOR ON command according to specified value.

FUNCTION

Under Apple mode only, this command is used to turn the FDD motor on or off. This is done by writing the /MOTOR ON mode control bit in the specified drive. After the /MOTOR ON command has been sent to the FDD, the FDC will monitor the /READY status line to verify that the command was completed. At the completion of the command, the FDC will issue a normal termination interrupt.

MO = "0"	Motor OFF
MO = "1"	Motor ON

ERROR CONDITIONS

If the /Ready line is not asserted within 1 second after the command is asserted, the FDC should abort the command and issue an interrupt. When the interrupt is asserted, the FDC should mark the command as abnormally terminated and assert the EC bit in the Status register 0 (ST0). The host will then issue a Sense Interrupt Status command to be read the EC bit.

Phase	R/W	D7 D6 D5 D4 D3 D2 D1 D0	Remarks
command	W	0 0 0 0 0 0 1 1	command code
	W	Step rate | Head Unload	
	W	Head load | ND	

FUNCTION

The Specify command is used to specify the initial values for several configuration parameters. There is no result phase and no error condition for this command.

PARAMETERS

STEP RATE

Under Apple mode, it is not necessary to specify the Step Rate, because the STEP command is fully handshaked with the FDD.

Under other modes, this Step Rate specifies the following interval of the step pulses generated by Seek, Recalibrate and Relative commands:

- for 2DD FDD with 250kbps TSRT = 2msec
- for 2DD FDD with 300kbps TSRT = 1.67msec
- for 2HD FDD TSRT = 1msec
- for 2ED FDD TSRT = 0.5msec
- for 2TD FDD TSRT = 0.4msec

Step Rate(16)	time
0	$16{*}T_{SRT}$
1	$15{*}T_{SRT}$
2	$14{*}T_{SRT}$
3	$13{*}T_{SRT}$
4	$12{*}T_{SRT}$
5	$11{*}T_{SRT}$
6	$10{*}T_{SRT}$
7	$9{*}T_{SRT}$

Step Rate(16)	time
8	$8{*}T_{SRT}$
9	$7{*}T_{SRT}$
A	$6{*}T_{SRT}$
B	$5{*}T_{SRT}$
C	$4{*}T_{SRT}$
D	$3{*}T_{SRT}$
E	$2{*}T_{SRT}$
F	$1{*}T_{SRT}$

HEAD UNLOAD TIME

Under Apple mode, it is unnecessary to specify this Head Unload time. Under other modes, this Head Unload specifies the following time to set the read/write head to unloaded state after the Read/Write group commands is executed:

- for 2DD FDD with 250kbps THUL = 2msec
- for 2DD FDD with 300kbps THUL = 1.67msec
- for 2HD FDD THUL = 1msec
- for 2ED FDD THUL = 0.5msec
- for 2TD FDD THUL = 0.4msec

Head Unload(16)	time	Head Unload(16)	time
0	Inhibited	8	$128 * T_{HUL}$
1	$16 * T_{HUL}$	9	$144 * T_{HUL}$
2	$32 * T_{HUL}$	A	$160 * T_{HUL}$
3	$48 * T_{HUL}$	B	$176 * T_{HUL}$
4	$64 * T_{HUL}$	C	$192 * T_{HUL}$
5	$80 * T_{HUL}$	D	$208 * T_{HUL}$
6	$96 * T_{HUL}$	E	$224 * T_{HUL}$
7	$112 * T_{HUL}$	F	$240 * T_{HUL}$

HEAD LOAD

Under Apple mode, it is unnecessary to specify the Head Load time. Under other modes, this Head load specifies the following stabilizing time of the read/write head after loading at the start of the Read/Write group commands:

- for 2DD FDD with 250kbps THLD = 2msec
- for 2DD FDD with 300kbps THLD = 1.67msec
- for 2HD FDD THLD = 1msec
- for 2ED FDD THLD = 0.5msec
- for 2TD FDD THLD = 0.4msec

Head Load(16)	time	Head Load(16)	time
00	Inhibited	08	$16*T_{HLD}$
01	$2*T_{HLD}$	09	$18*T_{HLD}$
02	$4*T_{HLD}$	⋮	⋮ HLD
03	$6*T_{HLD}$	⋮	⋮ HLD
04	$8*T_{HLD}$	⋮	⋮ HLD
05	$10*T_{HLD}$	7D	$250*T_{HLD}$
06	$12*T_{HLD}$	7E	$252*T_{HLD}$
07	$14*T_{HLD}$	7F	$254*T_{HLD}$

ND The ND (Non-DMA) field, when set to 1, specifies that the FDC will transfer data to the host in interrupt mode under all operational modes.

Write Data

Phase	R/W	D7 D6 D5 D4 D3 D2 D1 D0	Remarks
Command	W	MT FM TB 0 0 1 0 1	command code
	W	X X X X X HD DR1 DR0	
	W	Cylinder	
	W	Head	
	W	Sector	
	W	(Bytes/Sector) / Format Byte	
	W	Last Sector in Multi Sector Write	
	W	GSL(MFM) / don't care(GCR)	
	W	Data Length in Bytes	
Execution			data transfer between Host and FDD
	R	Status Regisiter 0	status information after this command
	R	Status Regisiter 1	
	R	Status Regisiter 2	
	R	Cylinder	
	R	Head	
	R	Sector	
	R	(Bytes/Sector) / Format Byte	

FUNCTION

The host can use this command to write sector data to the specified sector. After this command has been issued, the FDC begins reading the address header (or ID field). When all four bytes loaded during parameters, cylinder, head, sector and Number of data bytes in the sector, written at the command phase match the four bytes of the address header (or the ID field) from the disk, the FDC takes data from the processor byte-by-byte via the data bus and outputs it to the FDD.

After writing data into the current sector, the specified sector number is incremented by one, and the next data field is written into. The FDC continues this "Multi-sector write" operation until the issuance of a Terminal Count Signal or until the last sector is meet. If the Terminal Count Signal is sent to the FDC it continues writing into the current sector to complete the data field. If the host asserts the Terminal Count signal, while a data field is being written, the FDC will fill the remainder of the data field with zeros.

The Multi-sector Write operation of the FDC must support 1:n

interleaving on all formats and transfer rates. Multi-sector Write operations while recording in GCR can accommodate any interleaving including 1:1. (When writing data in GCR, the write-splice occurs after the bit-slip bytes)

TAG BYTES

For GCR format;

TB = 1	Data in the 12 Tag bytes should be transferred from the host.
TB = 0	Data in the 12 Tag bytes are automatically filled with zeroes.

ERROR CONDITIONS

1) When the FDC can not find the following within the 400msec for the GCR format, or when the FDC can not find out the following before two Index pulses are input for the MFM and FM format.

- Address Mark in the Address header (ID field)
- Desired Address header (Data in the ID field)

2) When the FDC detects the read error in the following:

- CRC bytes or the Checksum bytes in the address header (or ID field)
- Bit Slip bytes only under GCR format

3) When the following conditions occur:

- WPRT_B pin becomes active
- Overrun or Underrun occur during the data transfer.
- When utilizing the TC input, it does not meet the correct timing period.
- Under Standard modes, the READY_B pin in the drive interface is inactive before this is operated under Standard modes.

Write Deleted Data

Phase	R/W	D7 D6 D5 D4 D3 D2 D1 D0	Remarks
command	W	MT FM 0 0 1 0 0 1	command code
	W	X X X X X HD DR1 DR0	
	W	Cylinder	
	W	Head	
	W	Sector	
	W	Number of data bytes in the Sector	
	W	Last Sector in Muliti Sector Read	
	W	GSL	
	W	Data Length in Bytes	
Execution			data transfer between Host and FDD
Result	R	Status Regisiter 0	status information after this command
	R	Status Regisiter 1	
	R	Status Regisiter 2	
	R	Cylinder	
	R	Head	
	R	Sector	
	R	Number of data bytes read	

FUNCTION

This command is used under Standard modes only and can not be supported under Apple mode. DAM and DDAM explained in the Write Data functions under standard modes are replaced with DDAM and DAM, respectively.

Phase	R/W	D7 D6 D5 D4 D3 D2 D1 D0	Remarks
command	W	MT FM SK 1 0 1 1 0	command code
	W	EC X X X X HD DR1 DR0	
	W	Cylinder	
	W	Head	
	W	Sector	
	W	Number of data bytes in the Sector	
	W	Last Sector in Muliti Sector Read	
	W	GSL	
	W	Data Length in Bytes	
Execution			data transfer between Host and FDD
Result	R	Status Regisiter 0	status information after this command
	R	Status Regisiter 1	
	R	Status Regisiter 2	
	R	Cylinder	
	R	Head	
	R	Sector	
	R	Number of data bytes read	

FUNCTION

This command is used under Standard modes.

This command has the same function as the Read Data command except that the DMA controller is set to the verify mode to transfer no data from the FDC to the host and to response the only DMAAK_B signal for the DMARQ signal without the active RD_B signal.

Version

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
command	W	0	0	0	1	0	0	0	0	command code
Result		1	0	0	1	0	0	0	0	Echo back for this command.

FUNCTION

This command is used under Standard modes. This command echoes back the "90H" at the result phase.

Chapter 5 Interface Timings

5.1.1 Host System Interface Timing

The host system interface timing diagrams for each command are shown in Figs.5.1-1 to 5.1-10. On the host side, in Command phase, check that RQM=1 and DIO=0 before writing data; in Result phase, check that RQM=1 and DIO=1 before reading data.

The timing of the READ DATA, READ ID, READ A TRACK, and RAW DUMP commands are shown in Fig.5.1-1.

• COMMAND PHASE

With the condition that RQM=1 and DIO=0, the RQM bit is reset when the command code is written to the data register of the FDC from the host. However, when contents of the data register are transferred to the FDC's internal command register, the RQM bit is set again and writing of the next parameter will be requested to the host. When the HD,DR1 and DR0 bits are written from the host, then the RQM bit is reset. When those bits are transferred to the FDC's command register, the RQM bit is set, and writing of the next parameter will be requested.

The DIO bit remains 0 until the command code and all required parameters are written. Consequently, the host monitors the RQM bit for when it becomes 1, and writes parameters in sequence in response. However, upon receiving the last parameter, the FDC enters E-phase without setting the RQM bit. The FIFO is disabled during the command phase to retain compatibility with the µPD765, and to provide for proper handling of the " Invalid Command " condition.

• EXECUTION PHASE

The process differs depending on whether the data transfer mode is the Non-DMA mode (interrupt process) or the DMA mode. After reset, the FIFO is disabled (FIFO Depth = 1). The FIFO is available only in the Execution Phase of the FDCs operation. The CONFIGURE command is used to enable the FIFO and also set the FIFO threshold. After reset, each data byte is transfered then by an INT or DRQ depending on the DMA mode. For more information on DMA modes and FIFO operations, please refer to FIFO Operations in section 5.1.2.

In the interrupt process, first the DIO bits is set to 1, and when the first data of the data field read from the disk is set in the data register, the RQM bit is set and an INT request is output. After receiving the INT request, the host confirms that both the RQM and DIO bits are 1, then reads the contents of the data register. When the contents of the data register are read, the FDC

resets the RQM bit. In the same way, the data transfer is performed until the last data is transferred. When that data is read by the host, the DIO bit is reset after reset of the RQM bit.

When this process is performed in the DMA mode, before entering C-phase the host sets the data transfer direction in the DMA controller by program. In E-phase, the FDC outputs the DRQ signal each time the FDC sets data read from the disk to the data register. Upon receiving the DRQ signal, the host carries out the following sequence; it returns the DACK_B signal, outputs the RD_B signal, reads the contents of the data register, stores the contents in memory, and stops the DACK_B signal. When the DACK_B signal is input from the host, the FDC resets the DRQ signal.

In Execution phase, the RQM and DIO bits remain reset. When the last data is transferred, Execution phase terminates. At this time the FDC set the result status and the parameters to the internal register, outputs the INT signal to request the host to read those data, and enters R-phase. The NDM bit(D5) of the status register is then reset.

• RESULTANT PHASE

The FDC first sets the DIO bit, and when contents of the ST0 register have been transferred to the data register, the FDC sets the RQM bit and requests reading of the contents (the result status ST0) of the data register. Upon receiving the INT signal, the host confirms that both the DIO and RQM bits are 1, then reads the contents (ST0) of the data register. When the contents of the data register are read, the RQM and DIO bits are reset, then the INT signal is reset. After reading the ST0, the host waits until the DIO and RQM bits become 1, then reads the result status ST1. In this way, when all necessary result status (ST0, ST1, and ST2) and parameters (C, H, S, and N) are read from the FDC, the FDC sets dummy data, then sets the RQM bit and waits for the next command.

The FIFO is disabled during the resultant phase to retain compatility with the μPD765. The resultant parameters of the executed command are immediately available, without the FIFO.

The timing of the WRITE DATA, FORMAT A TRACK, and FORMAT/WRITE commands are shown in Fig.5.1-2. This timing is the same as that of the Read Data group commands except for the different data transfer direction (DIO=0) in Execution phase.

The timing of the SENSE DRIVE STATUS command is shown in Fig. 5.1-3. In the Command phase, only the command code and data specified by the HD, DR1, and DR0 bit are written. There is no Execution phase for this command. In the Resultant phase, the INT signal is not output; therefore after Command phase, the host side confirms that both the DIO and RQM bits are 1, then reads the contents of the ST3 set to the data register and terminates command execution.

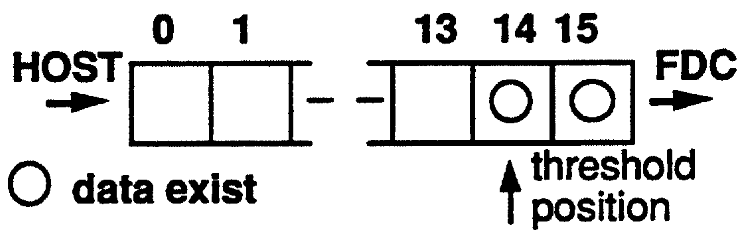
parameters,the FDC clears any FIFO data to ensure the validity, and enters into the execution phase. In execution phase, the FDC can support the single and demand transfer, and allow the system some latency defined by threshold value When the data transfer terminates normally or abnormally, the FDC enters into the result phase.At the beginning of result phase, the INT signal is generated. For each command, a defined set of result bytes has to be read from the FDC. The result byte may be read from the FDC after RQM=1 and DIO=1 of status register. When the HOST read the all parameters, the status register of FDC becomes RQM=1, DIO+0,CB=0,and result phase end.

5.1.2 1 FIFO Threshold

In using the FIFO, the HOST is allowed a large service latency without causing a overrun or underrun error. The user can program this latency to adjust his purpose. THRESHOLD is defined as the number of available bytes to the FDC until the HOST starts to service the data from a FDC request (i.e.DMARQ is active).

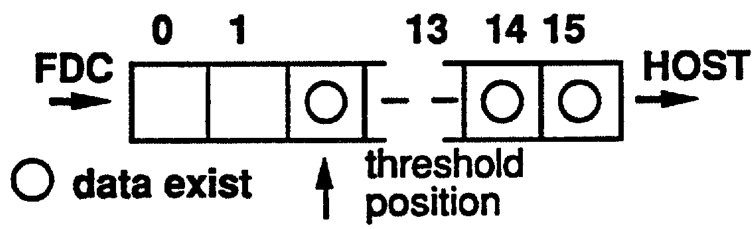
ex: FIFO STATES WHEN DMARQ BECOMES ACTIVE (THRESHOLD=2)

FROM HOST TO FDC



The FDC takes out data bytes from the FIFO. When two data bytes are left in the FIFO, the FDC will activate the DMARQ. and request service from the HOST.

FROM FDC TO HOST



The FDC takes data bytes into the FIFO. When the number of data bytes in the FIFO is 14 (the open cells are two), the FDC will activate the DMARQ and request service from the HOST.

Fig.5.1-1 READ DATA, READ ID, READ A TRACK, and RAW DUMP Commands

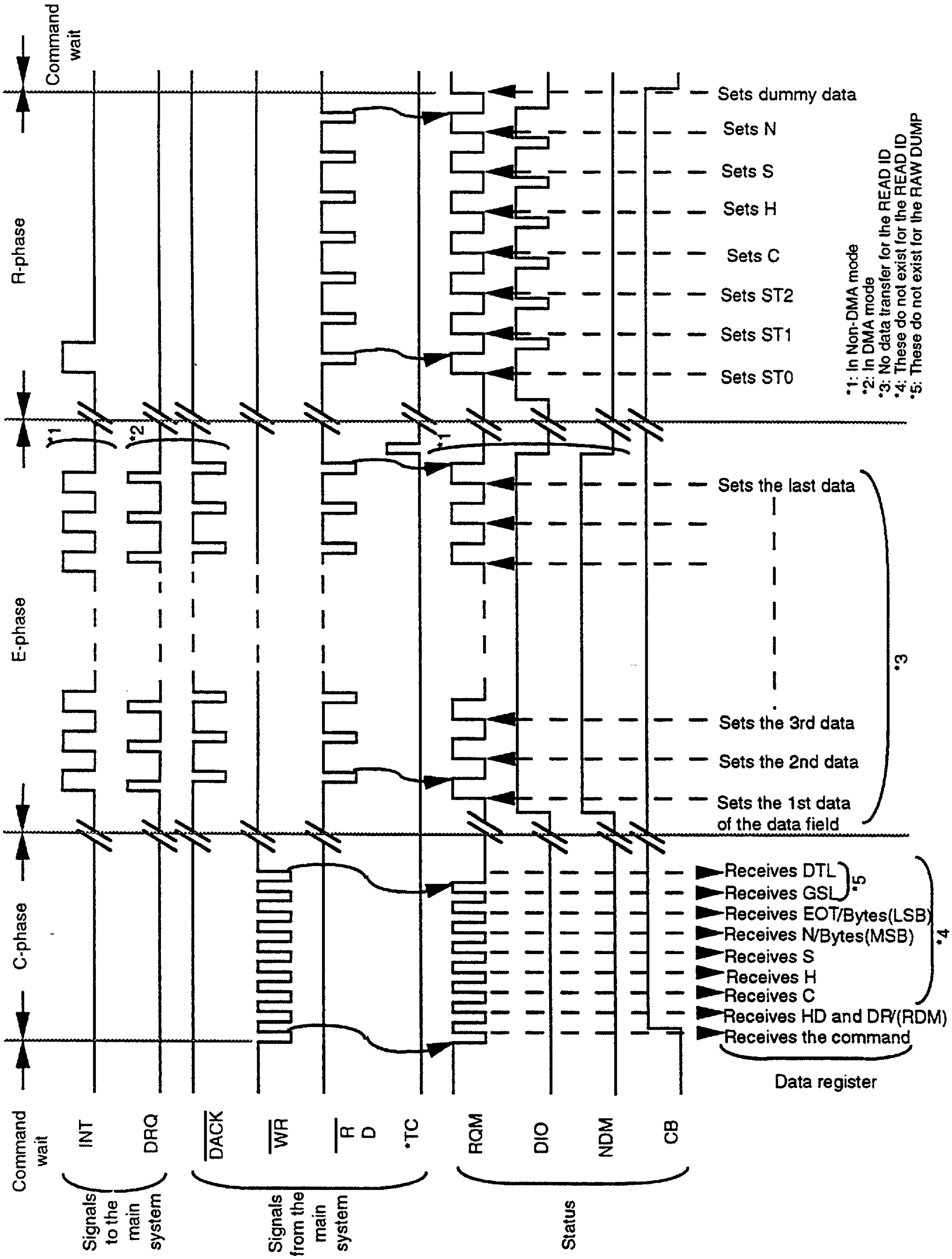


Fig.5.1-3 SENSE DRIVE STATUS command

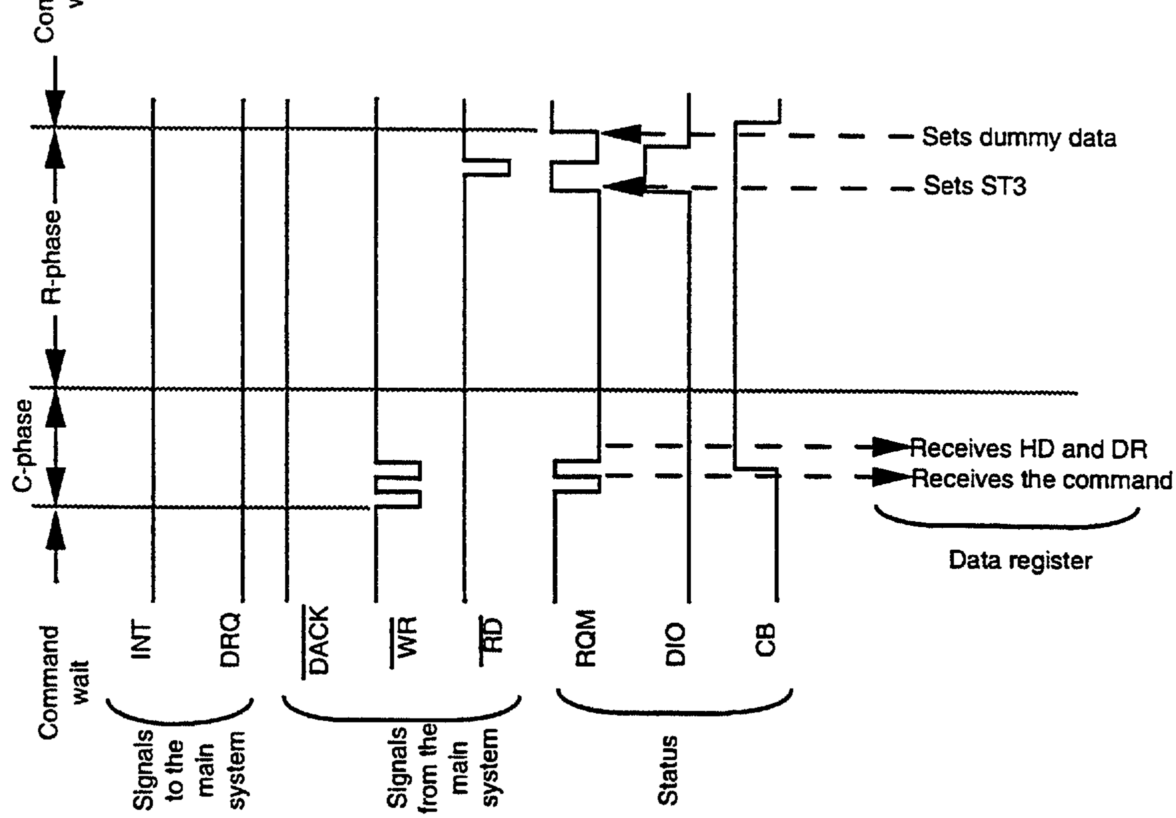
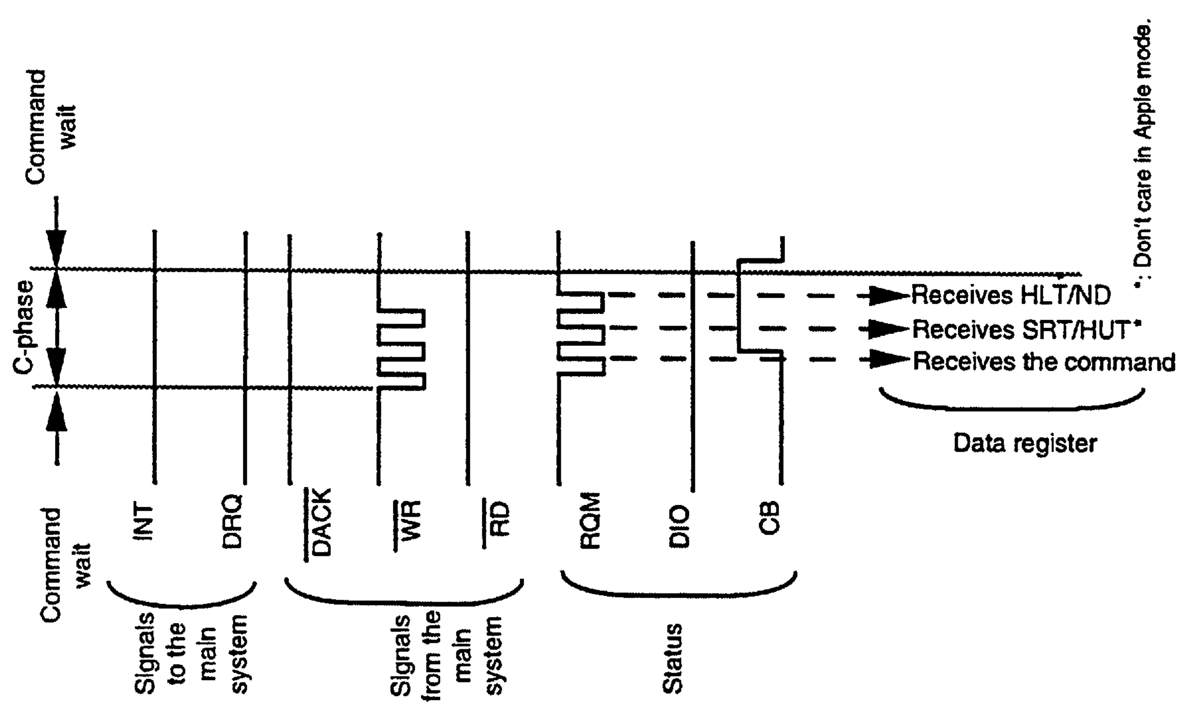
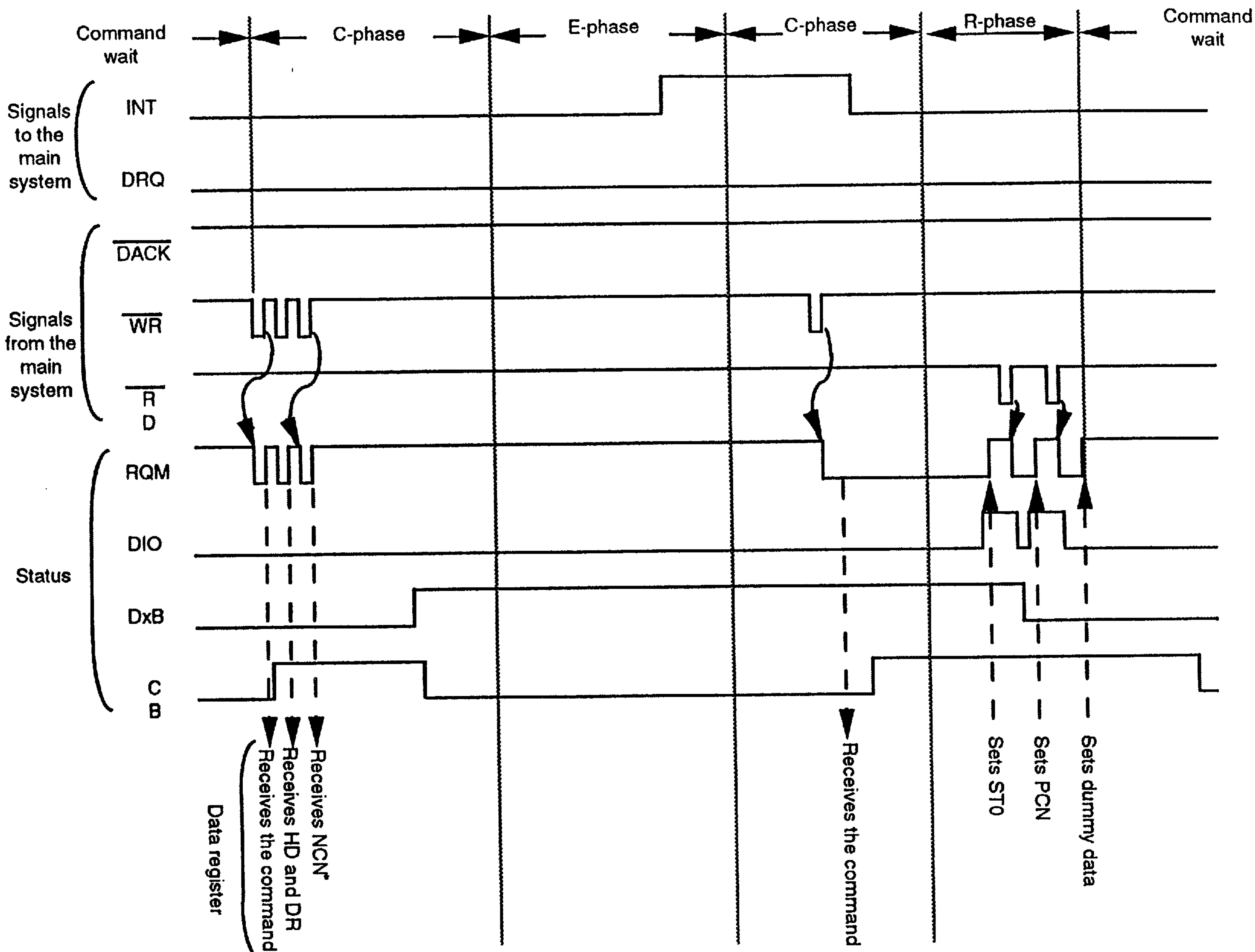


Fig.5.1-4 SPECIFY command





*: This does not exist for RECALIBRATE

Fig.5.1-5 SEEK and RECALIBRATE commands **Fig.5.1-6 SENSE INTERRUPT STATUS command**

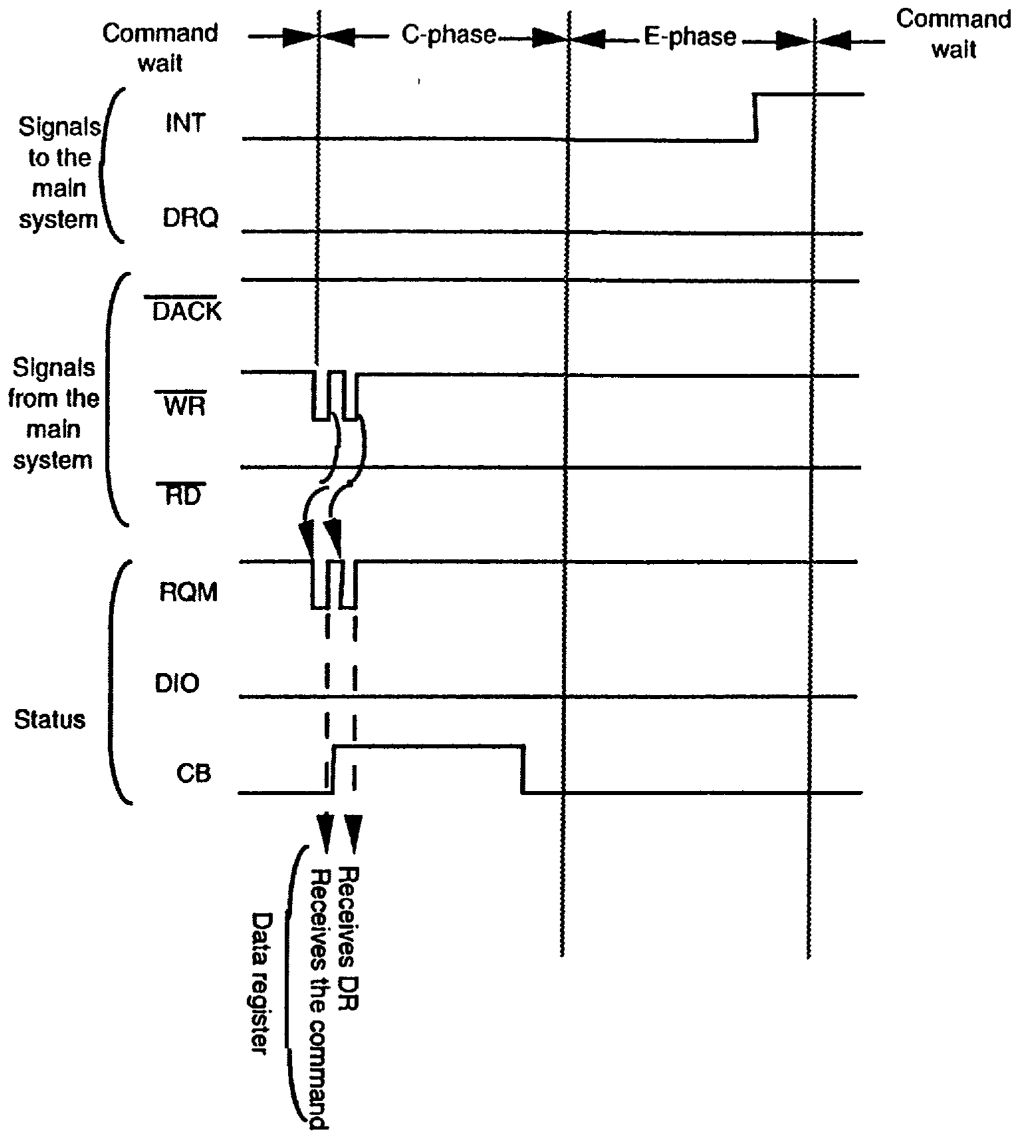


Fig 5.1-7 Disable/Enable DPLL, SET DRIVE MODE, SET MOTOR CONTROL and Set Enable Control commands

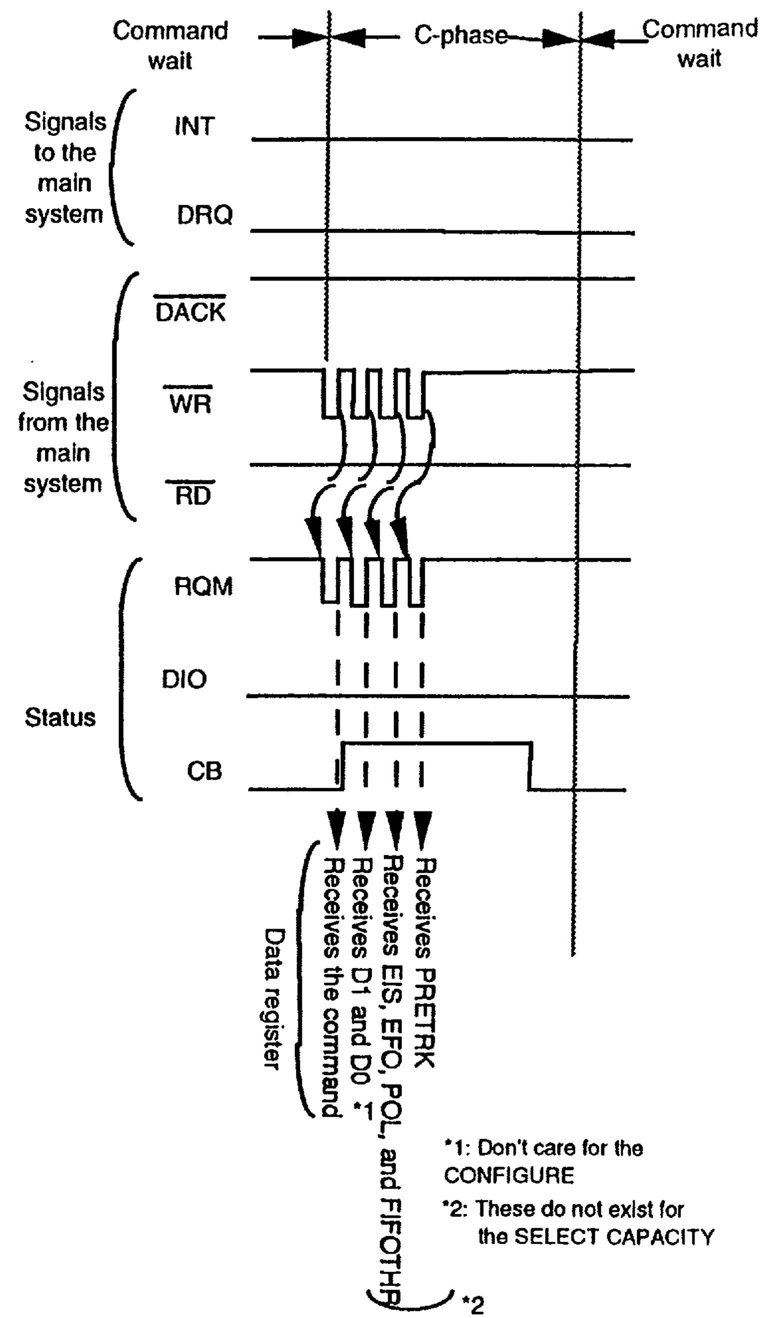


Fig.5.1-8 CONFIGURE and SELECT CAPACITY commands

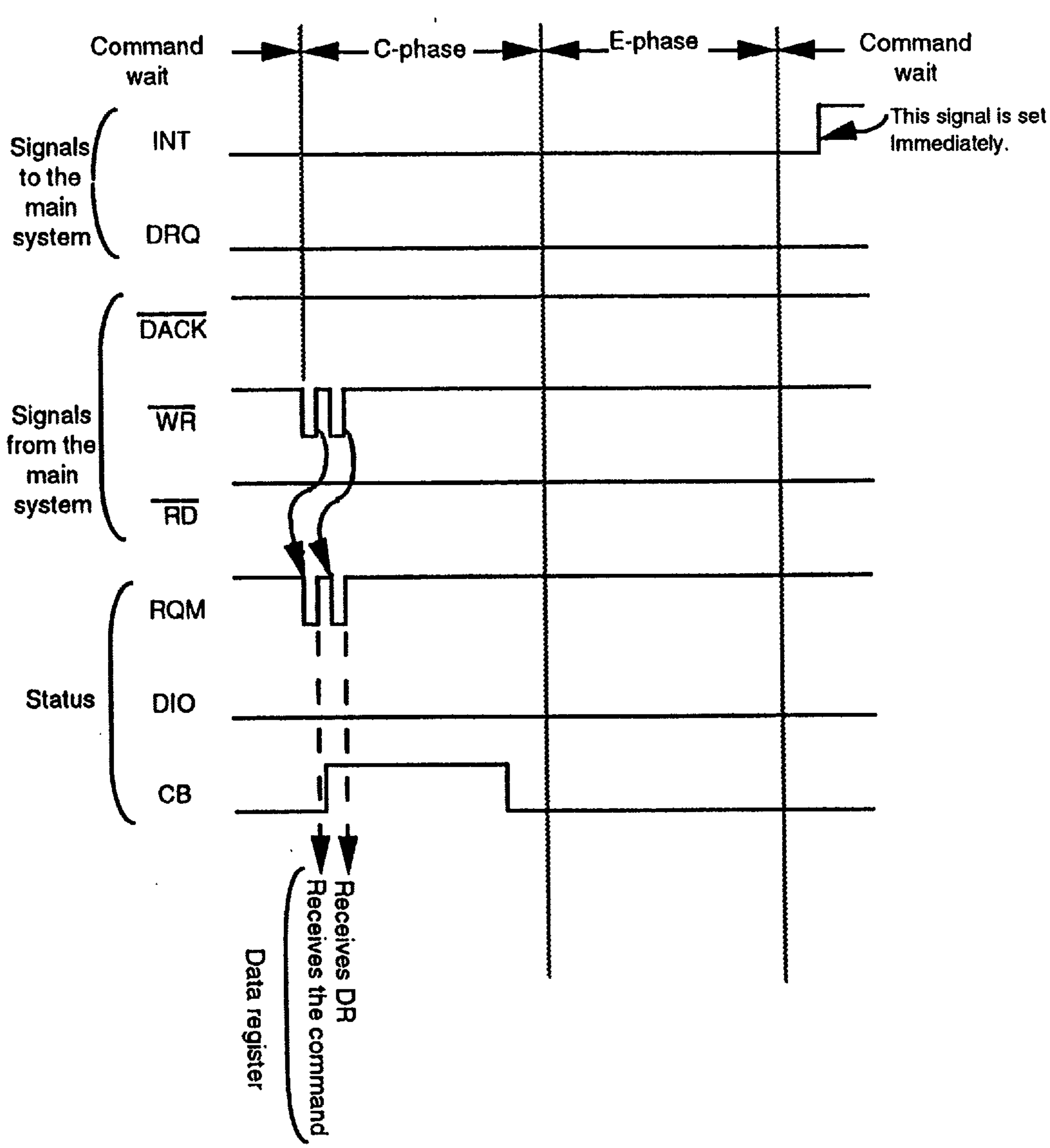


Fig.5.1-9 EJECT DISK command

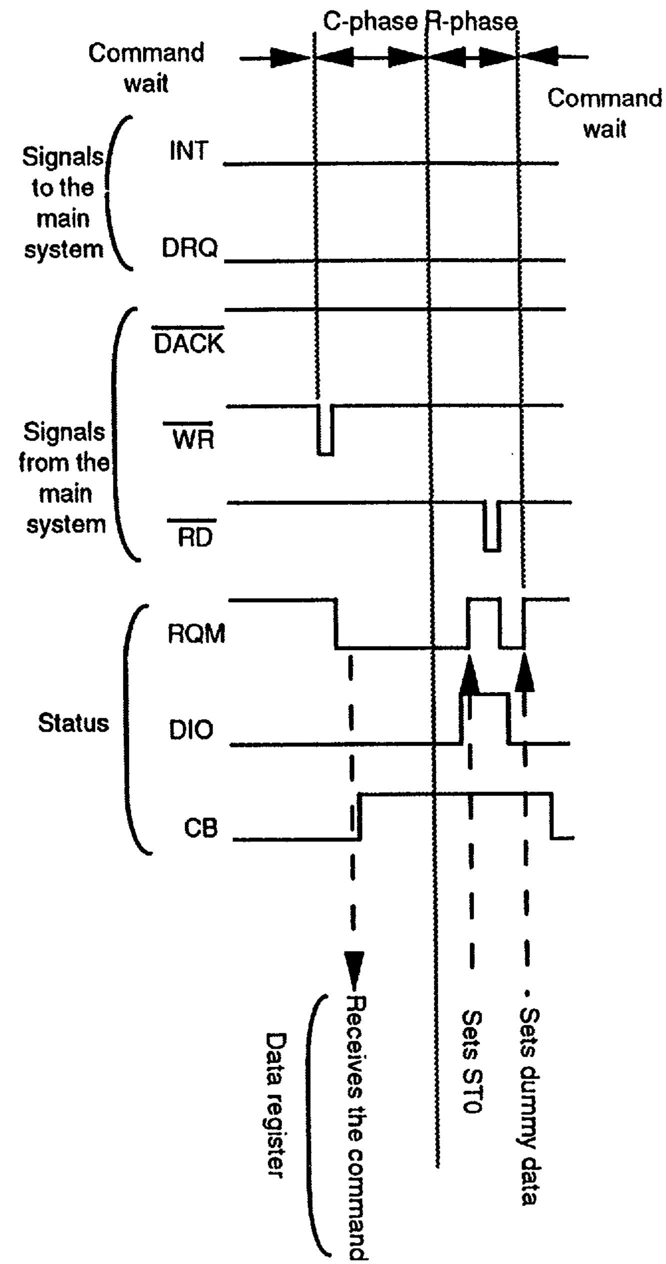
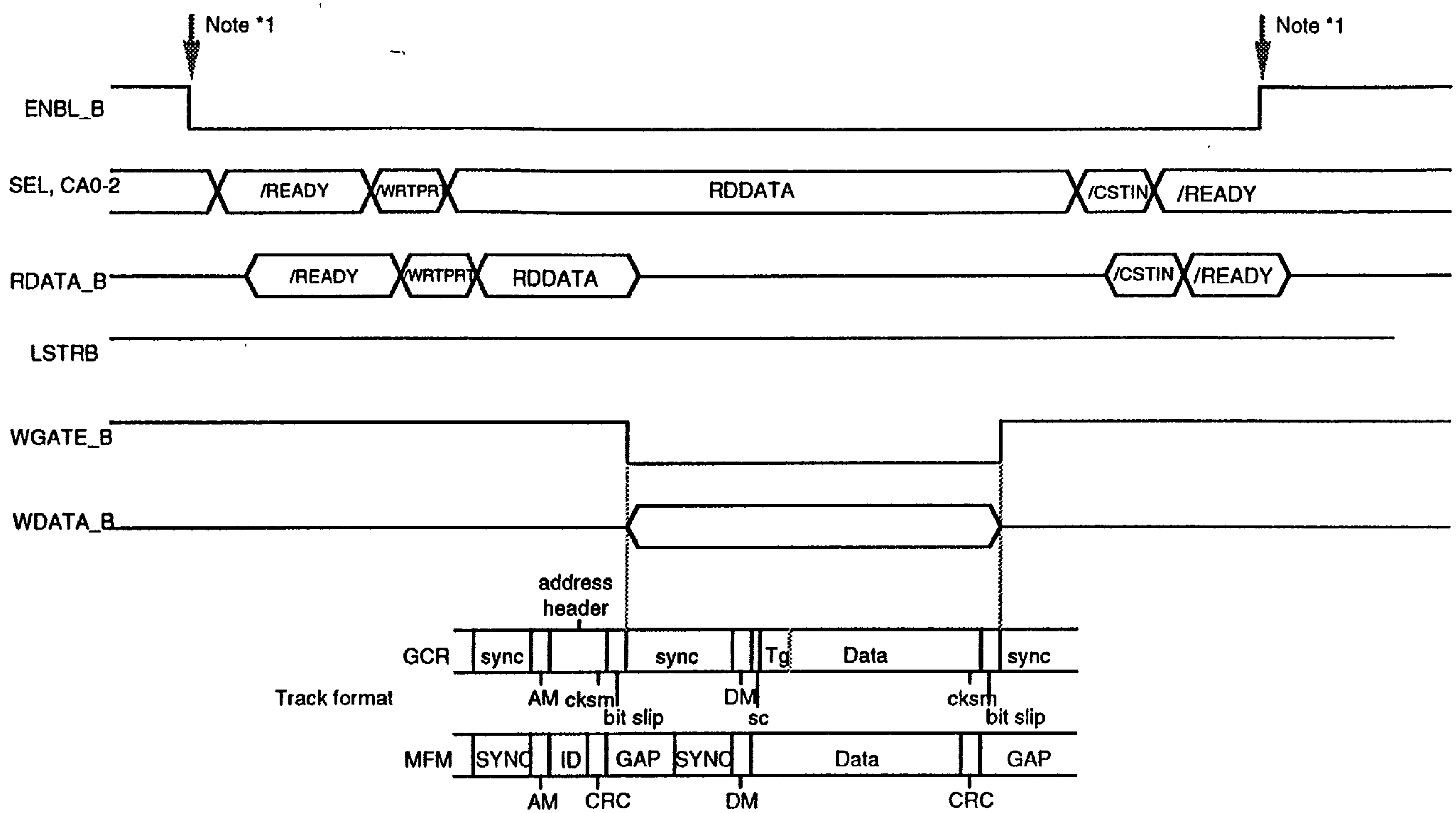


Fig.5.1-10 INVALID command

5.2 Drive Interface Timing

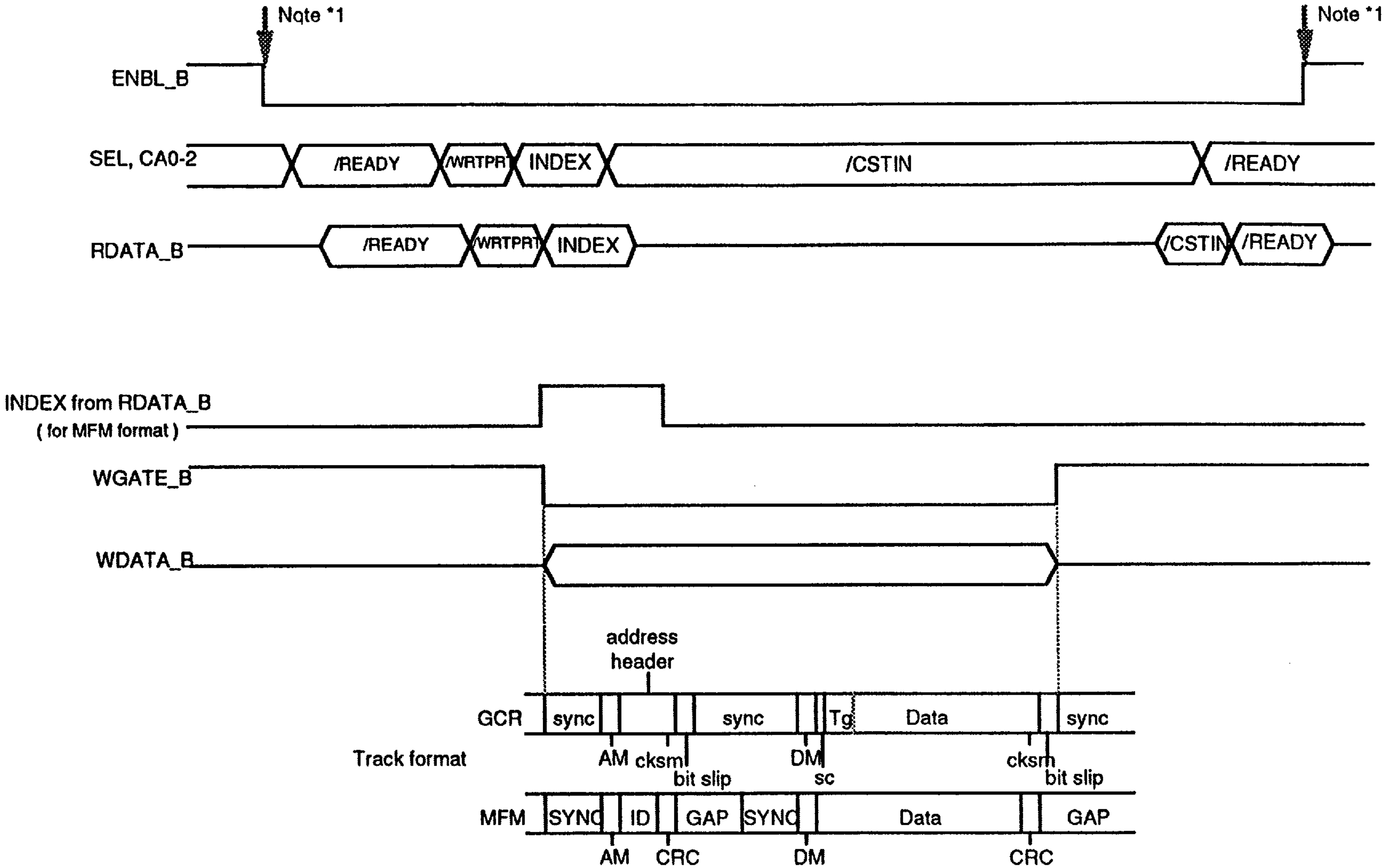
Under Apple mode, drive interface side timing diagrams for each command are shown from Fig. 5.2-1 to 5.2-10.

Under Standard modes, the Drive Interface timing is almost the same timing as that of the μPD765A.



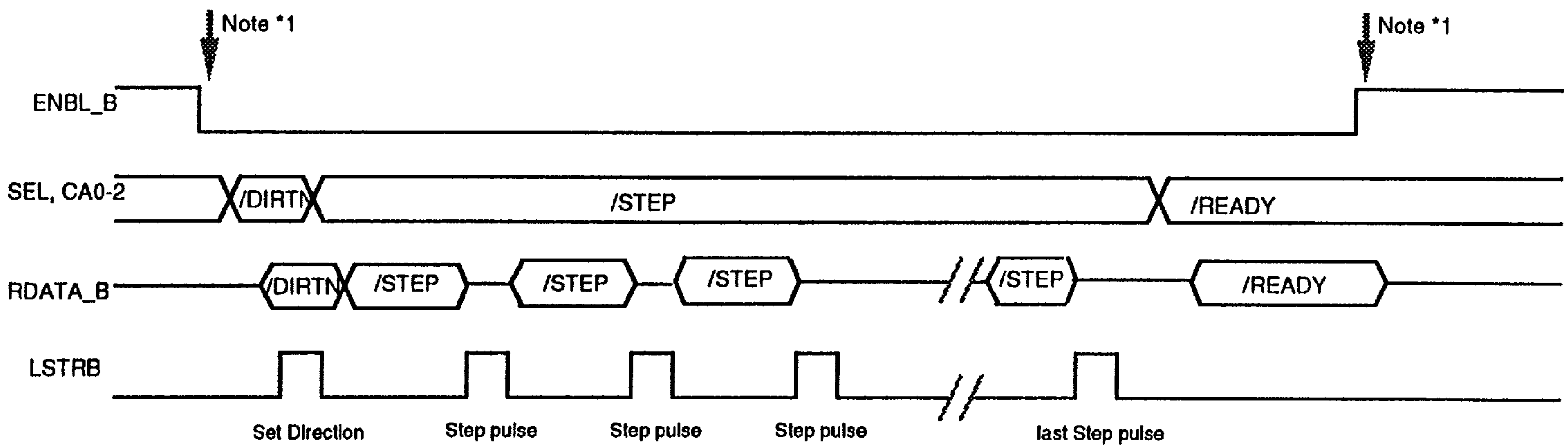
Note *1 : This signal can be controlled by the only "Set Enable Control" command.

Fig.5.2-2 WRITE DATA



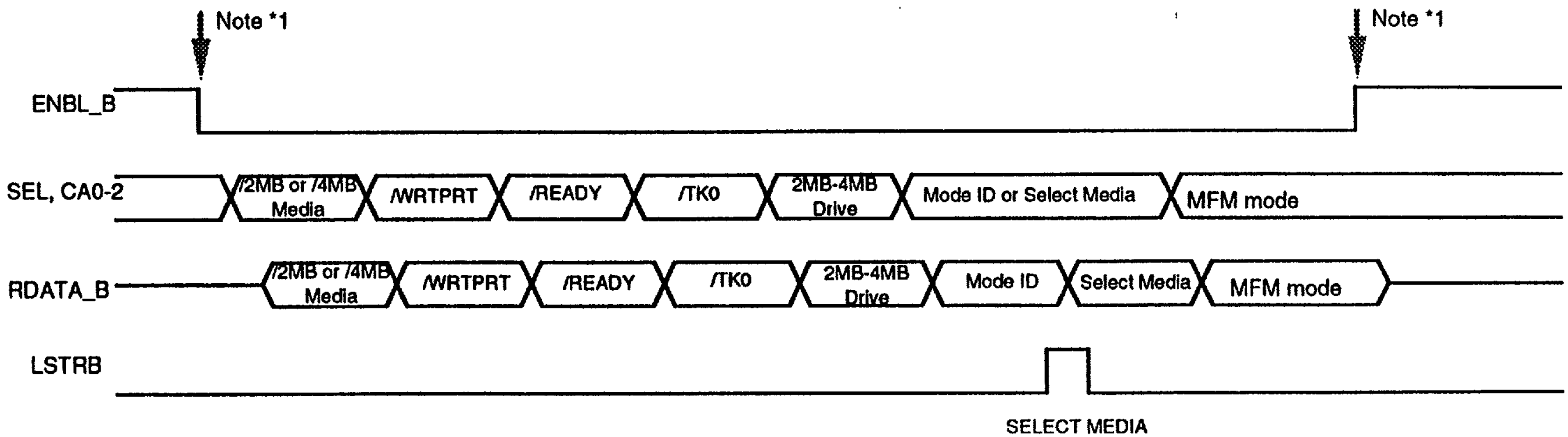
Note *1 : This signal can be controlled by the only "Set Enable Control" command.

Fig.5.2-3 FORMAT A TRACK and FORMAT/WRITE



Note *1 : This signal can be controlled by the only "Set Enable Control" command.

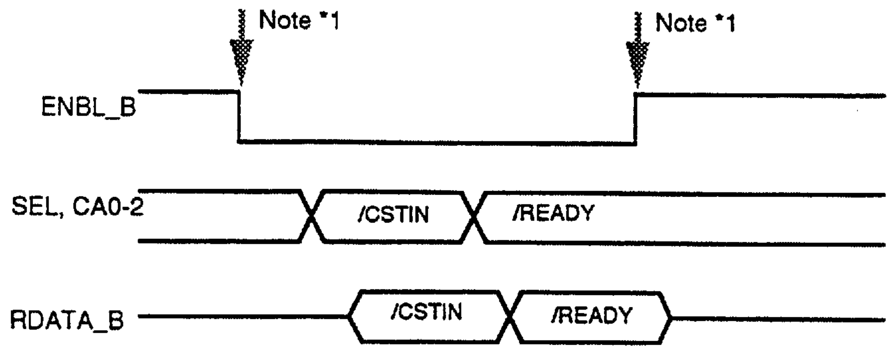
Fig.5.2-4 SEEK and RECALIBRATE



Note *1 : This signal can be controlled by the only "Set Enable Control" command.

Fig.5.2-5 SENSE DRIVE STATUS

Fig.5.2-6 SENSE INTERRUPT STATUS



Note *1 : This signal can be controlled by the only "Set Enable Control" command.

Fig.5.2-11 Set Motor Control for Motor OFF

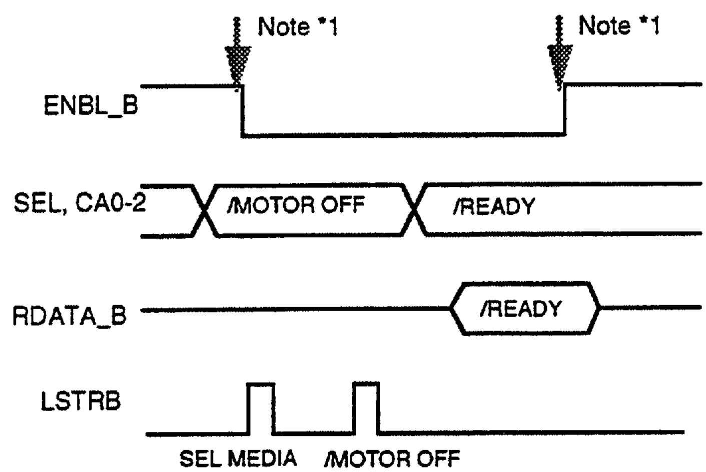
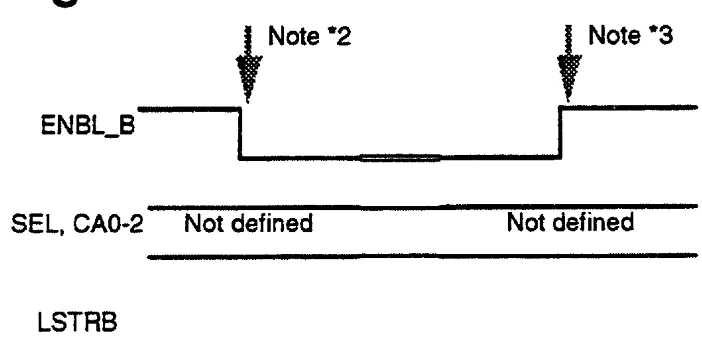
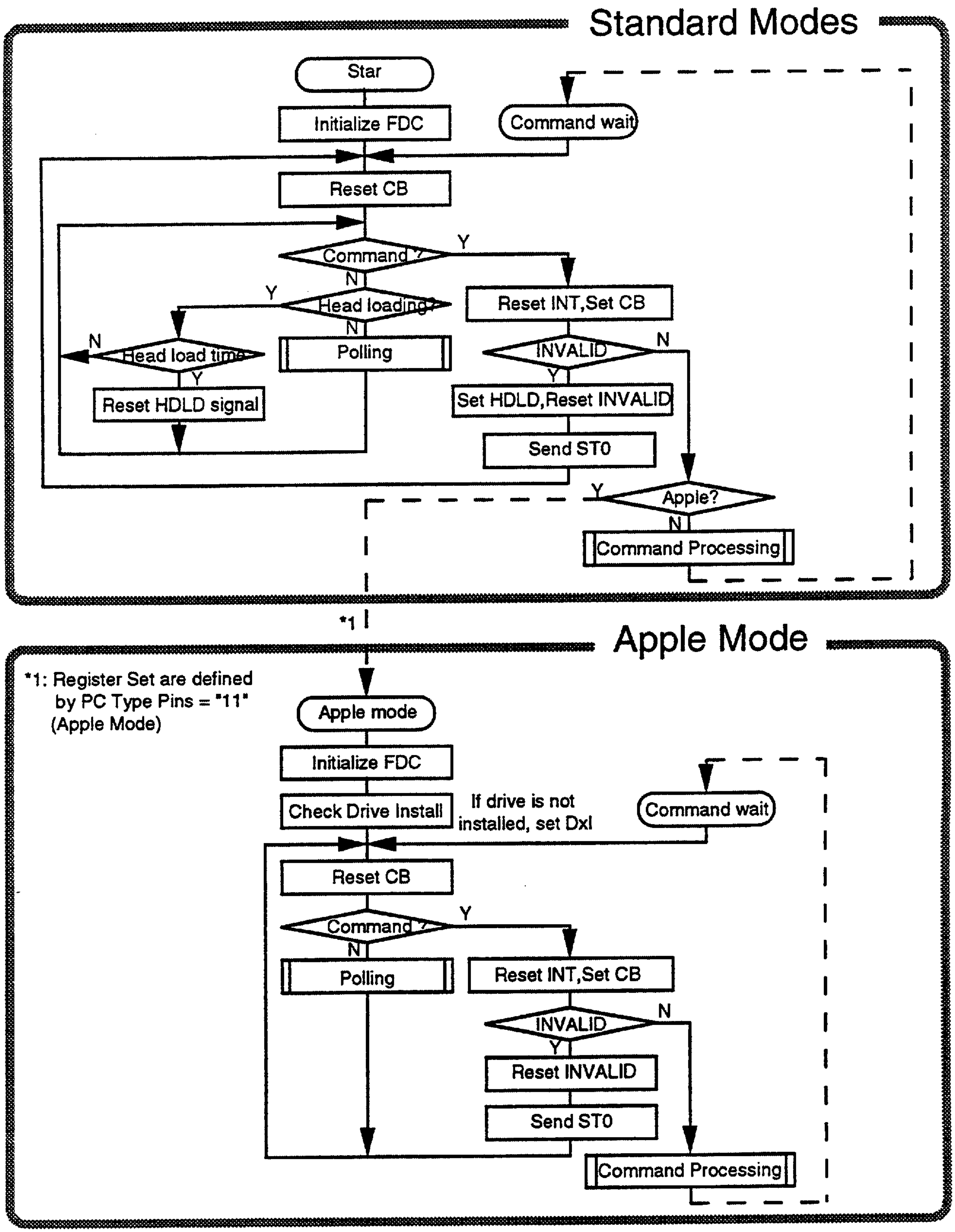


Fig.5.2-12 Set Enable Control

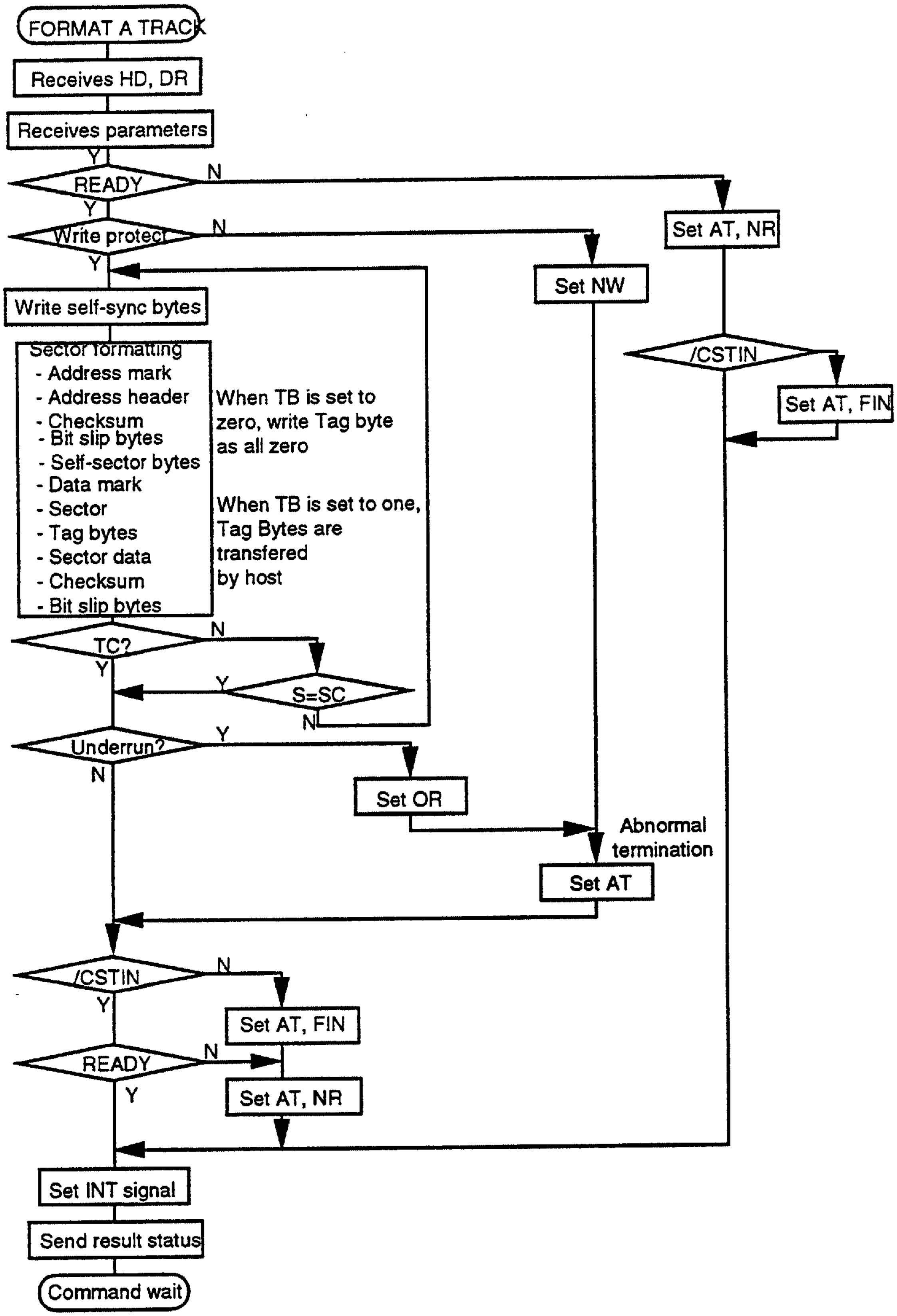


Note *1 : This signal can be controlled by the only "Set Enable Control" command.
Note *2 : The ENBL_B is set to the active state by the "Set Eanble Control"
Note *3 : The ENBL_B is reset to the inactive state by the "Set Eanble Control"

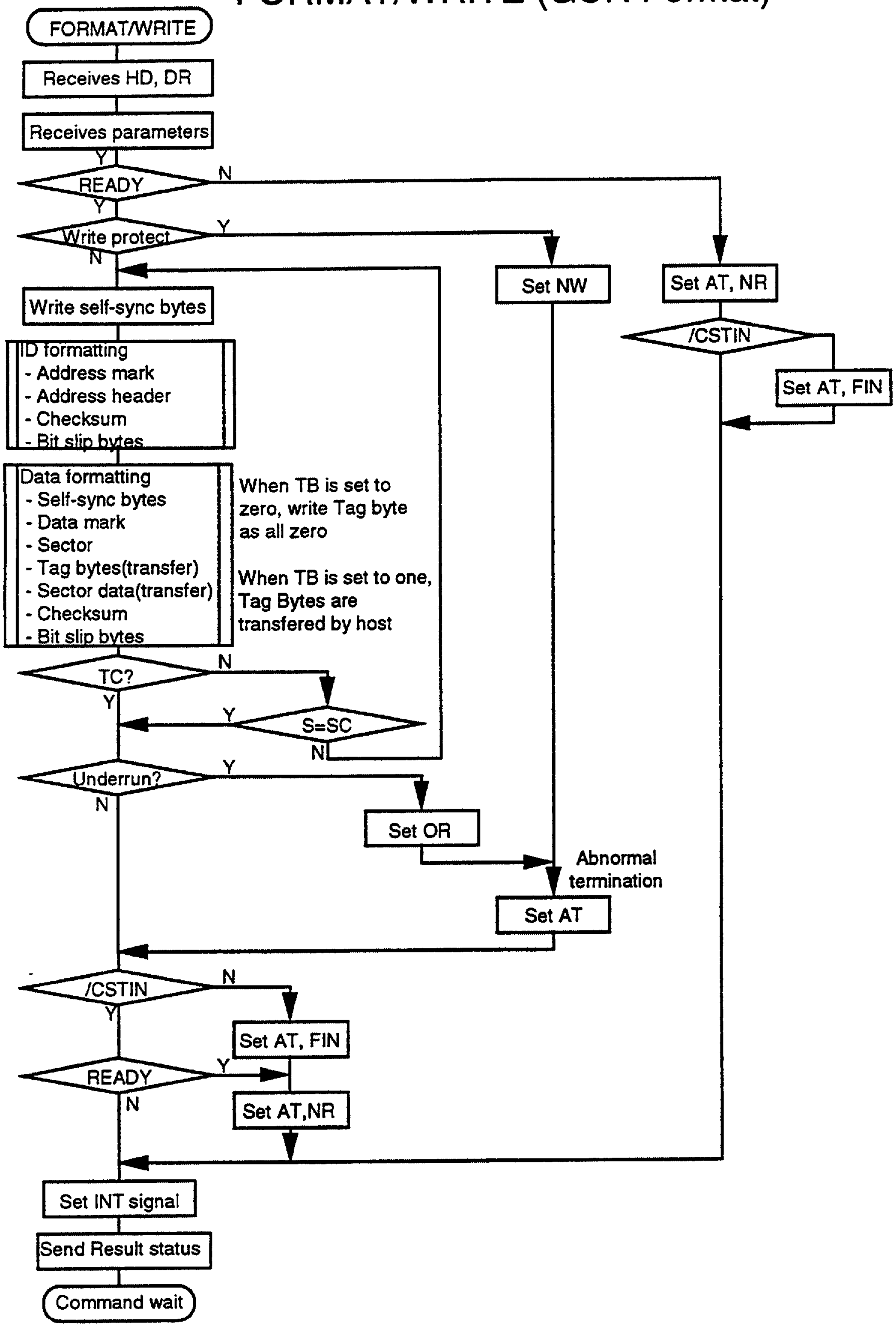
COMMAND WAIT STATE



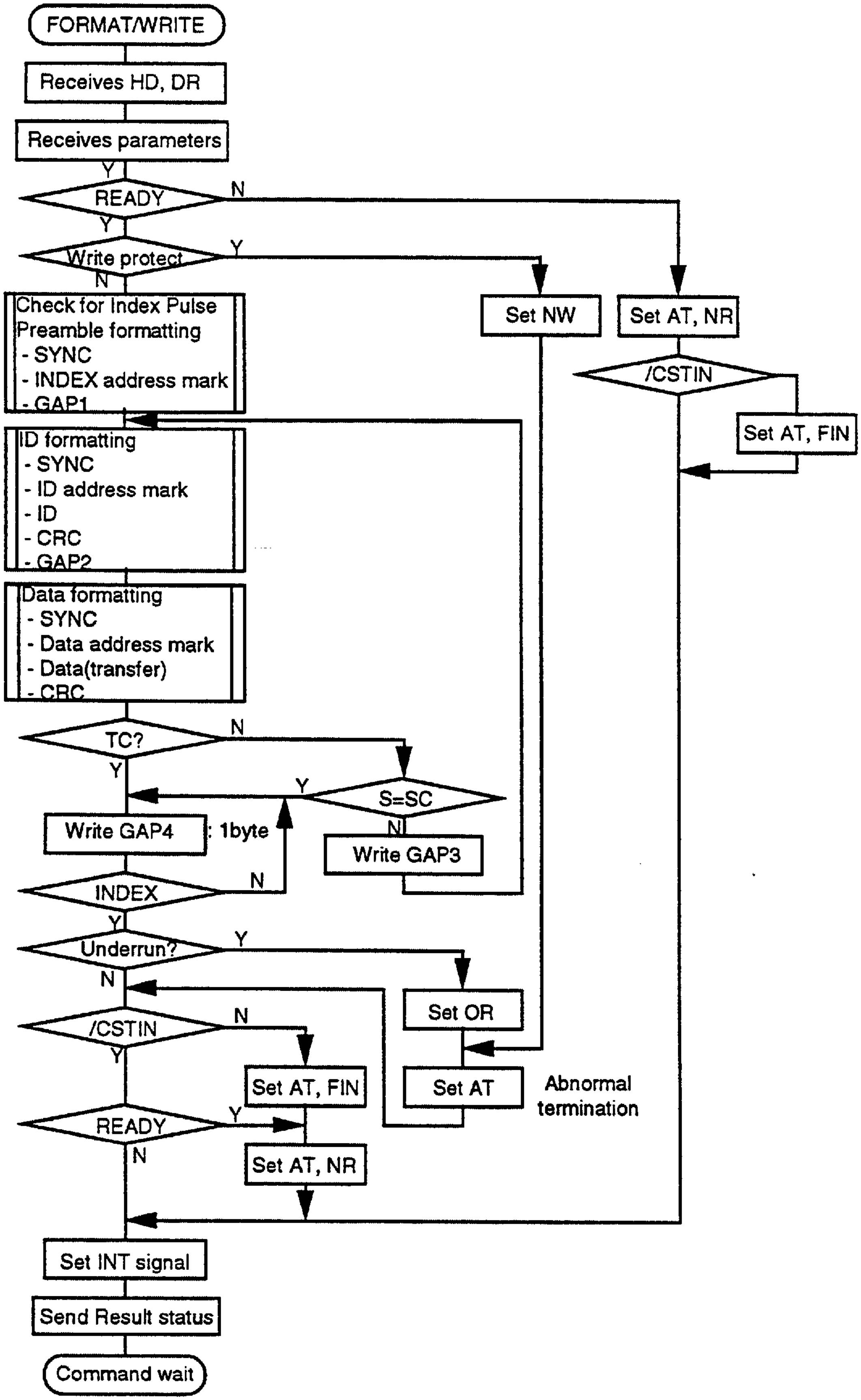
FORMAT A TRACK (GCR Format)



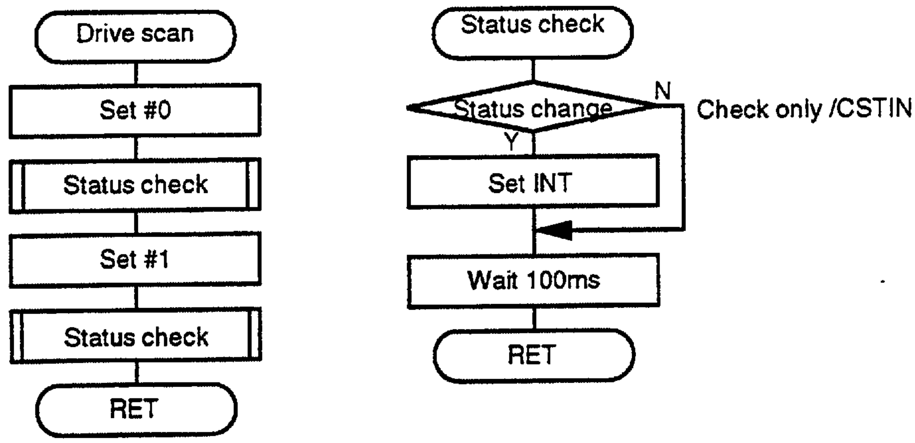
FORMAT/WRITE (GCR Format)



FORMAT/WRITE (MFM Format)

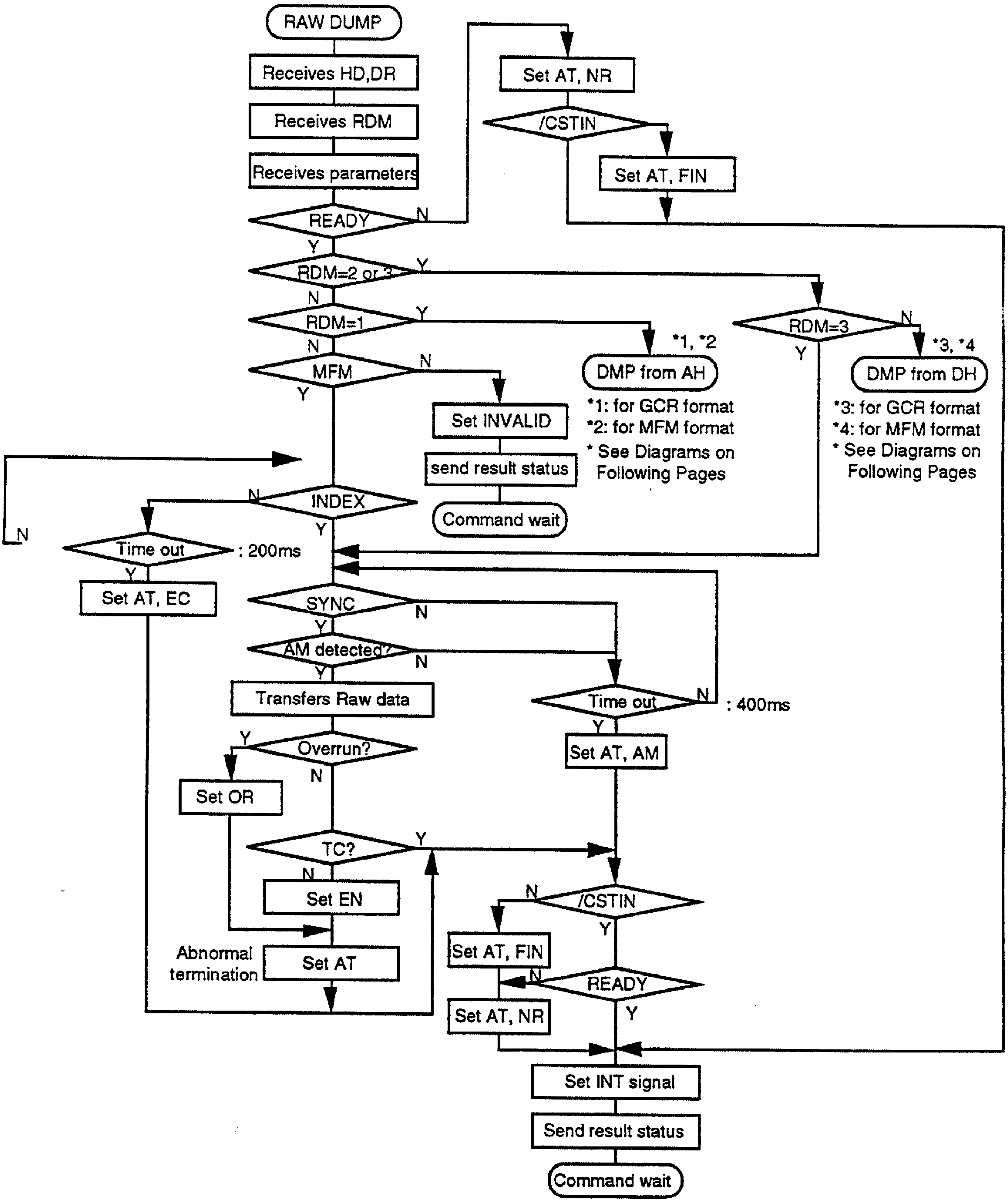


POLLING



Drive scan
Set #0
Status check
Set #1
Status check
RET
Status check
Status change
N
Y
Check only /CSTIN
Set INT
Wait 100ms
RET

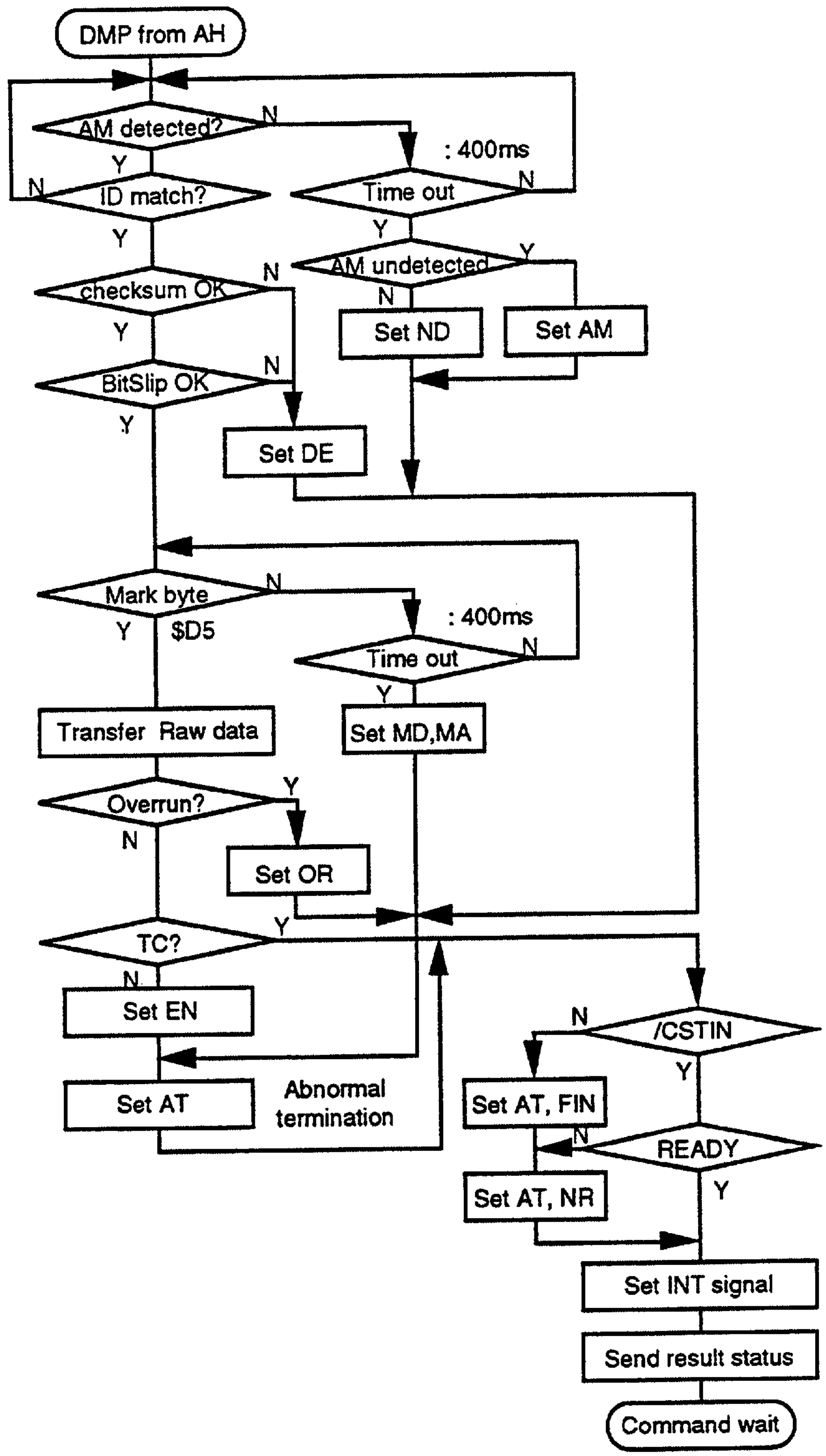
RAW DUMP



RAW DUMP
Receives HD,DR
Receives RDM
Receives parameters
READY
N
Y
Set AT, NR
/CSTIN
Set AT, FIN
RDM=2 or 3
Y
N
RDM=1
Y
N
RDM=3
N
Y
*1, *2
*3, *4
DMP from AH
DMP from DH
MFM
N
Y
Set INVALID
send result status
Command wait
*1: for GCR format
*2: for MFM format
* See Diagrams on Following Pages
*3: for GCR format
*4: for MFM format
* See Diagrams on Following Pages
INDEX
N
Y
Time out
: 200ms
Set AT, EC
SYNC
N
Y
AM detected?
N
Y
Transfers Raw data
Time out
N
: 400ms
Y
Set AT, AM
Overrun?
Y
N
Set OR
TC?
Y
N
Set EN
Abnormal termination
Set AT
/CSTIN
N
Y
Set AT, FIN
READY
N
Y
Set AT, NR
Set INT signal
Send result status
Command wait

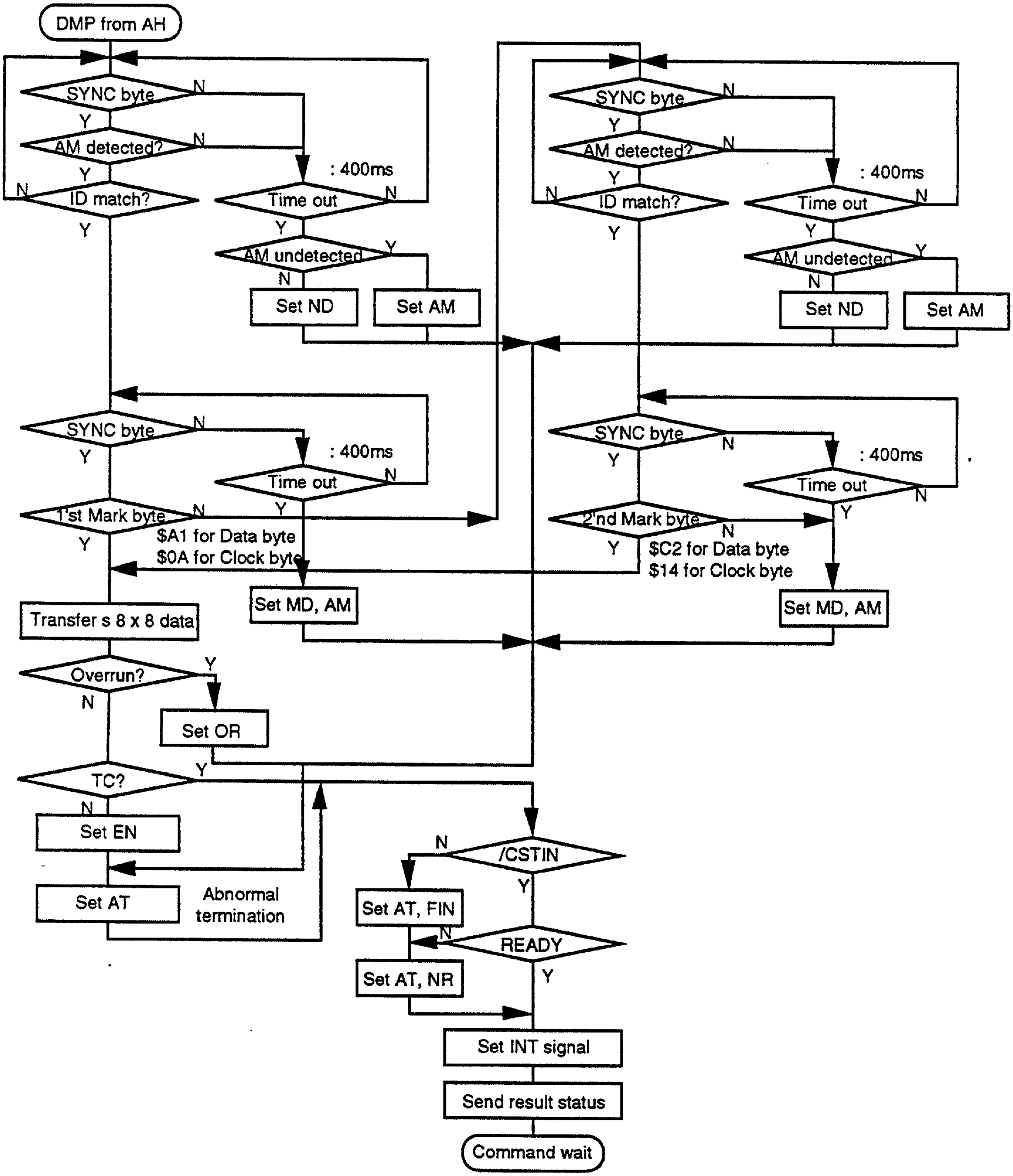
RAW DUMP

*1 : Dump from Address Header (GCR Format)



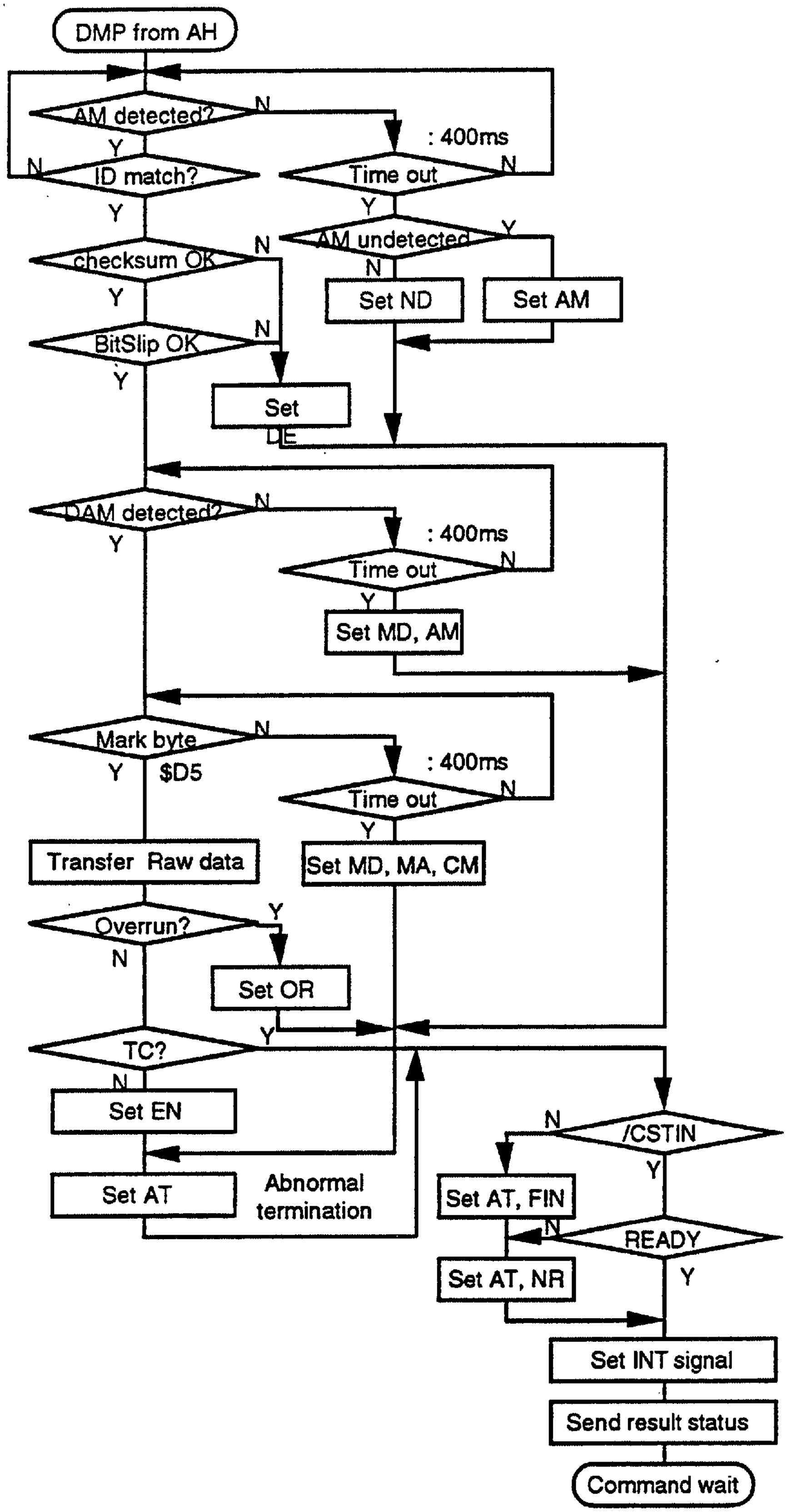
RAW DUMP

*2 : Dump from Address Header (MFM Format)



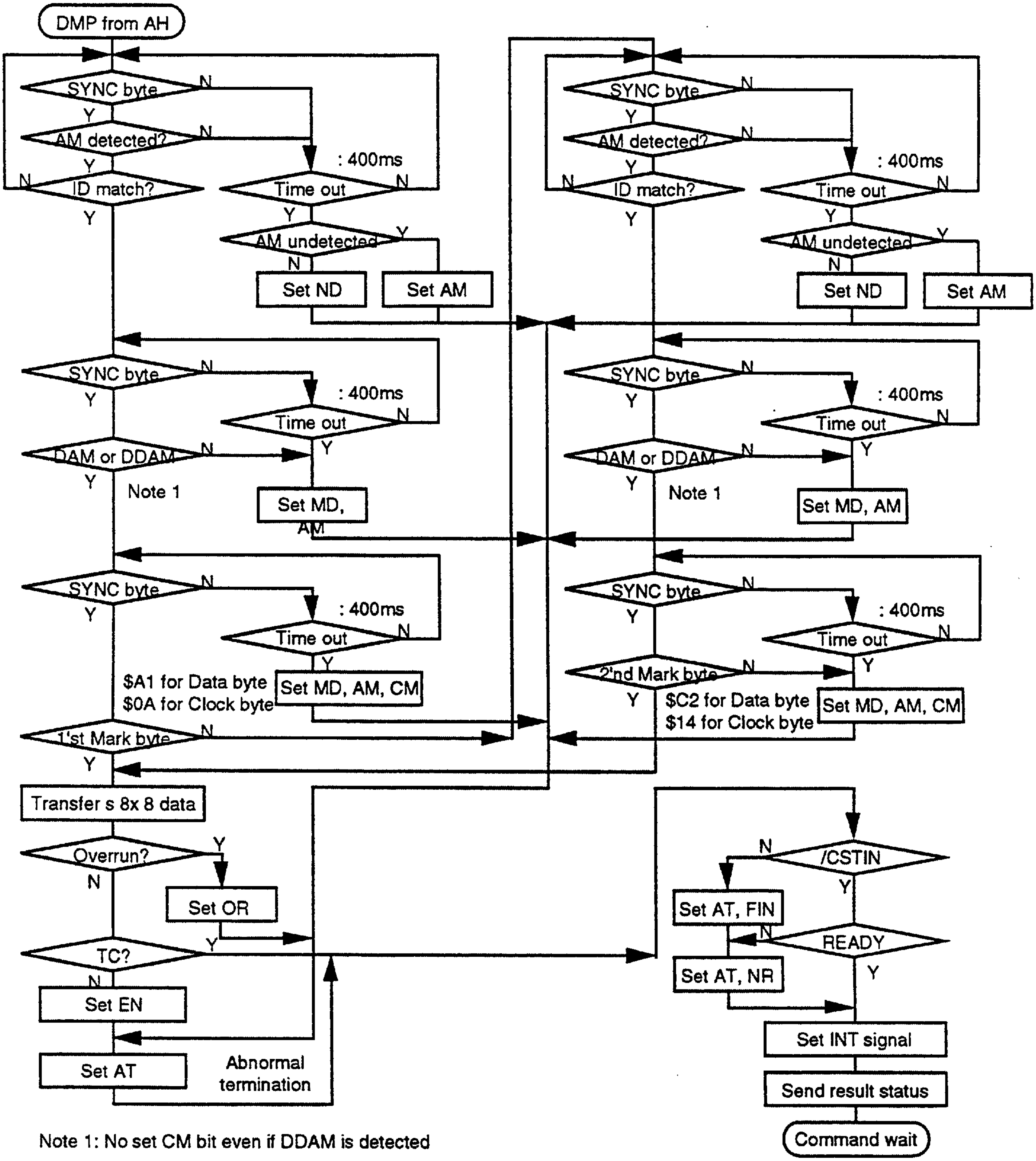
RAW DUMP

*3 : Dump from Data Header (GCR Format)



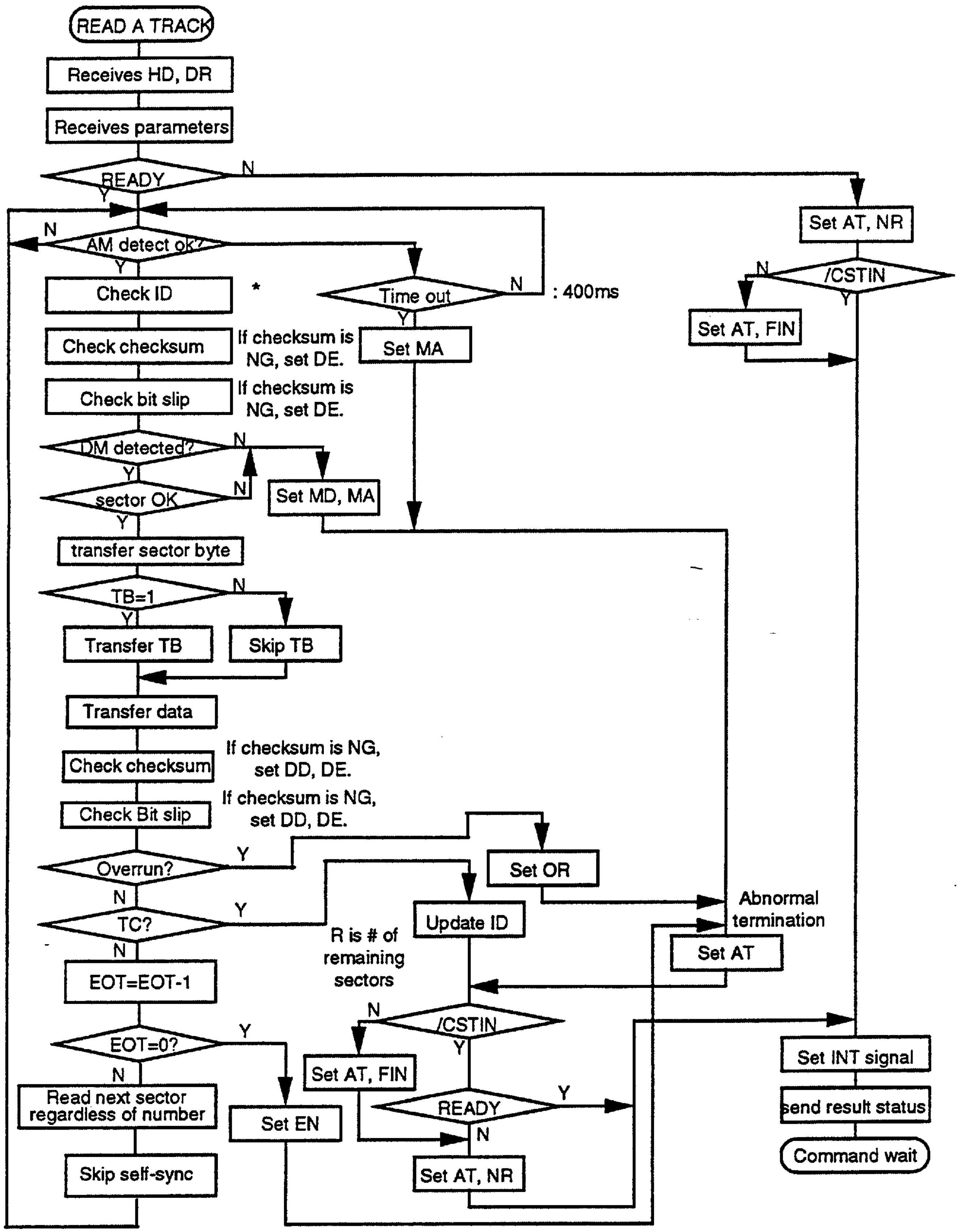
RAW DUMP

*4 : Dump from Data Header (MFM Format)



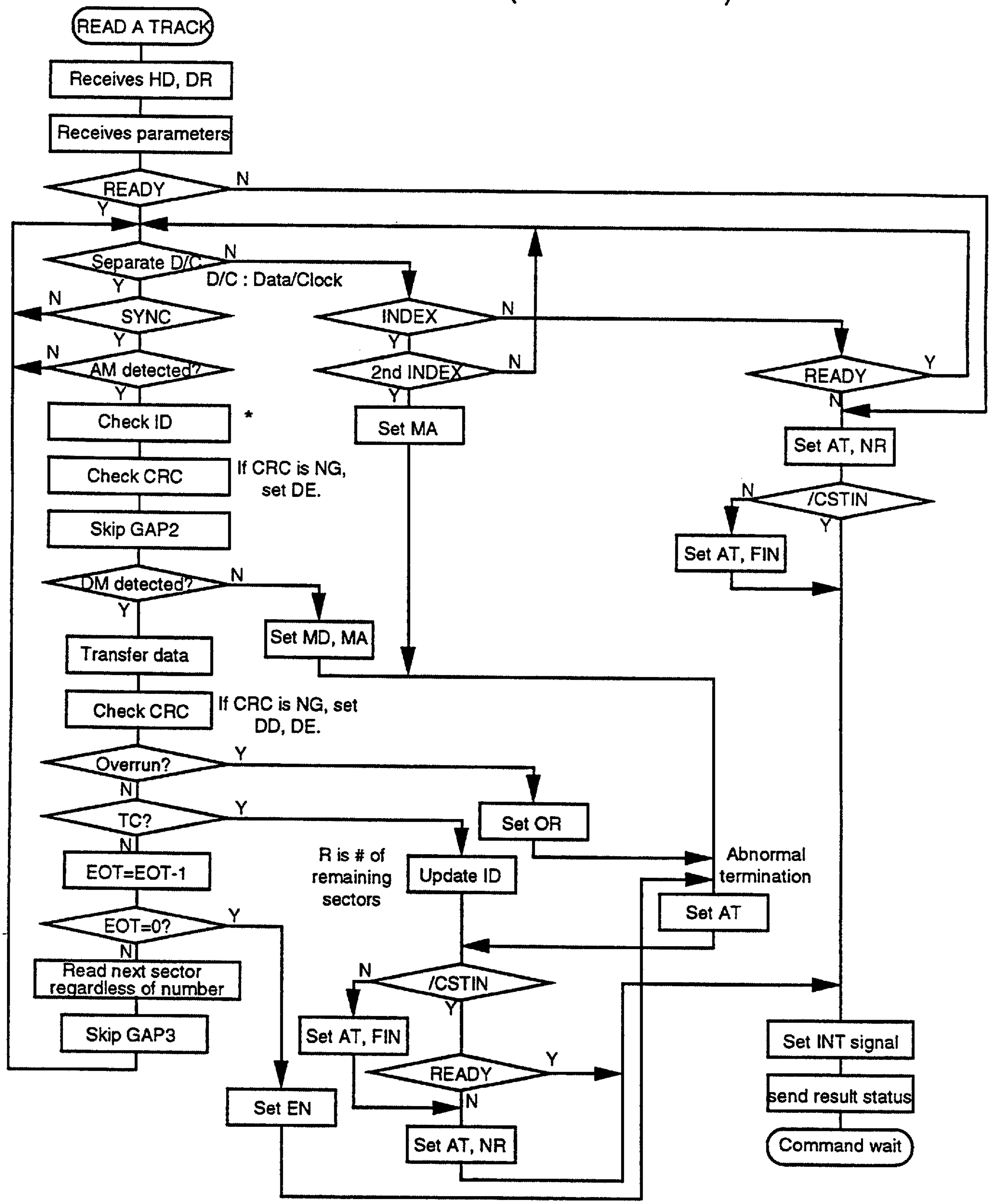
Note 1: No set CM bit even if DDAM is detected

READ A TRACK (GCR Format)



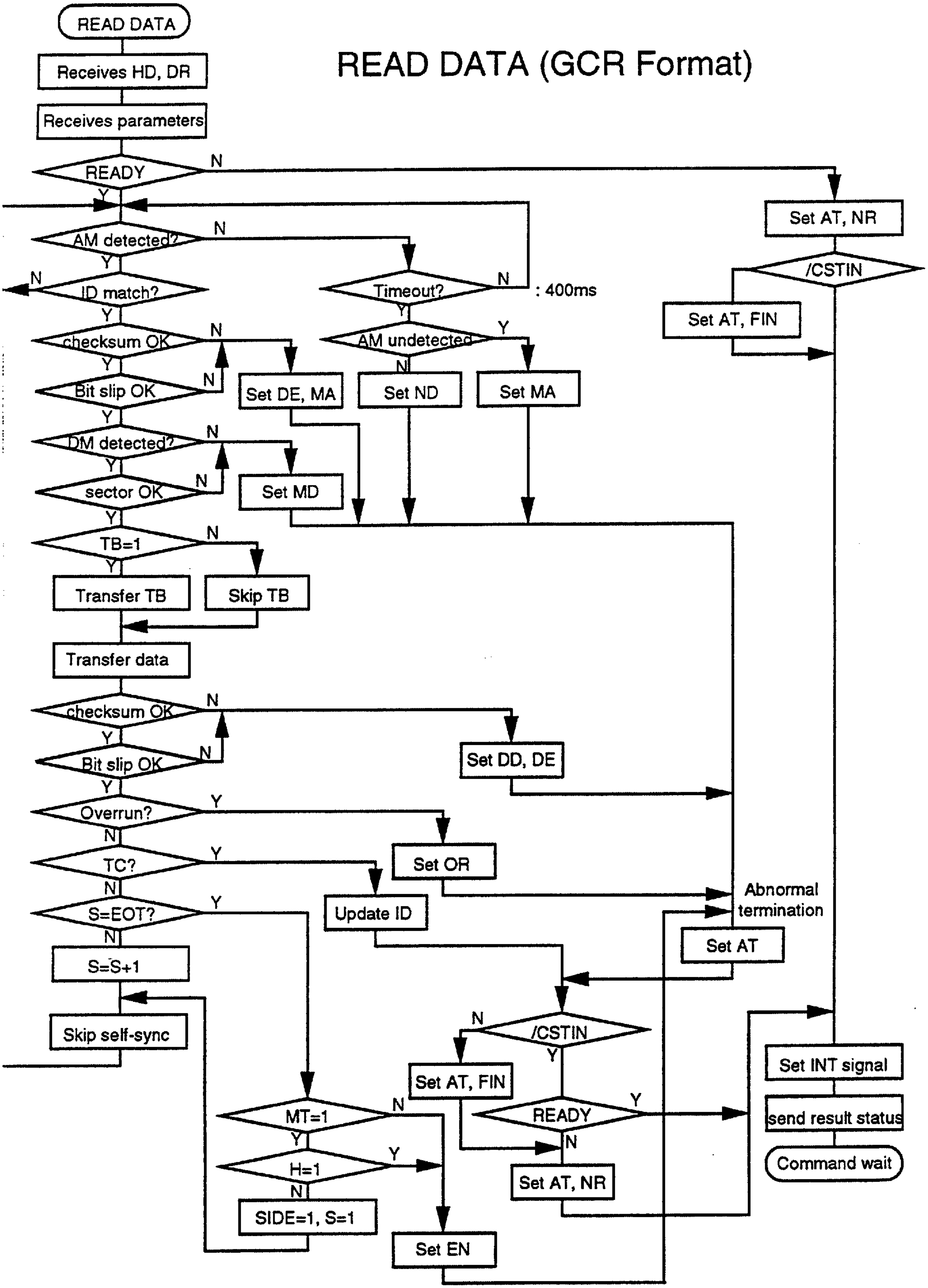
* : Search the specified sector at first. If it be couldn't find by time out, set ND and terminate. Since 2nd sector, check ID and set ND if the ID is NG , and continue the command processing.

READ A TRACK (MFM Format)

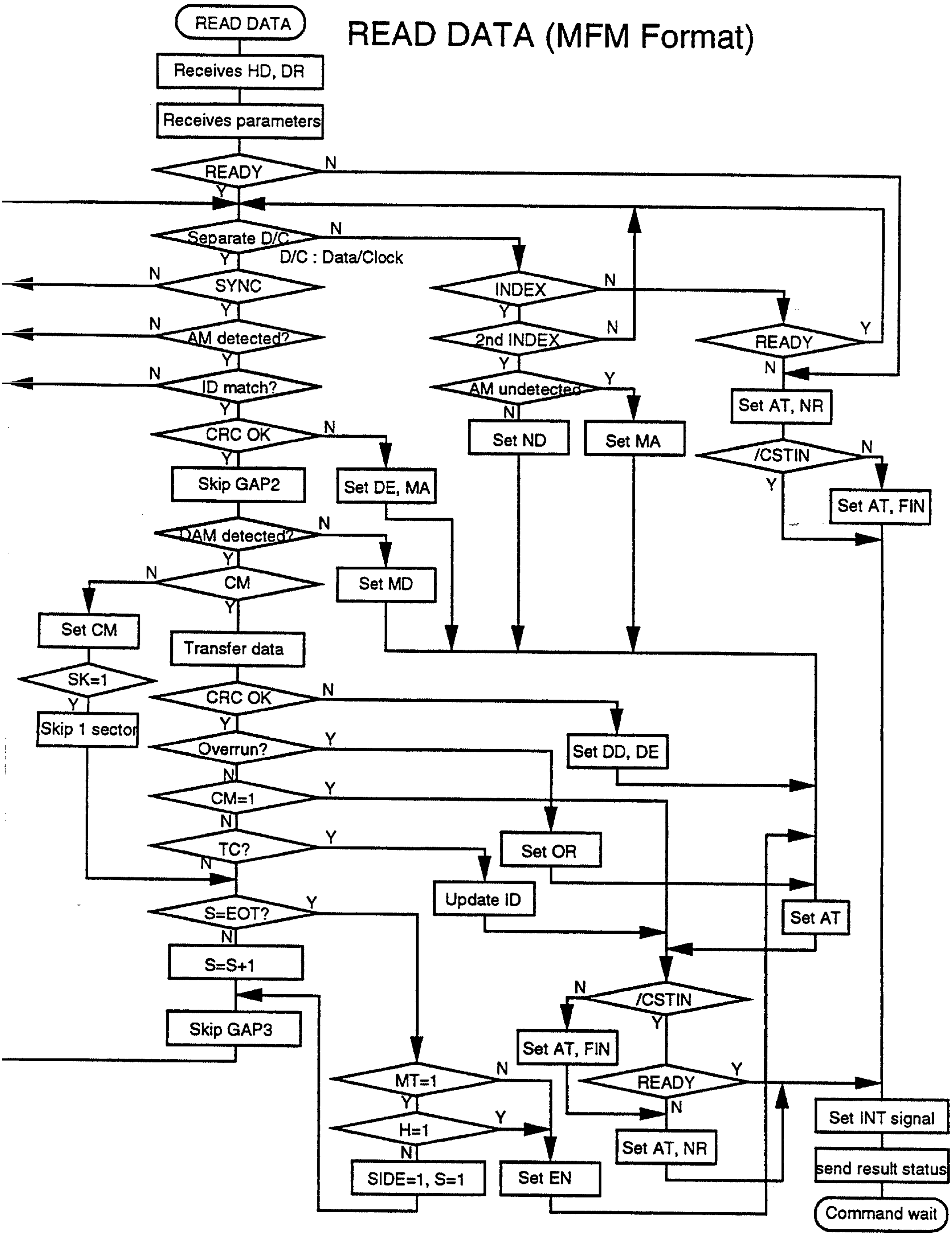


* : Search the specified sector at first. If it be couldn't find by time out, set ND and terminate. Since 2nd sector, check ID and set ND if the ID is NG, and continue the command processing.

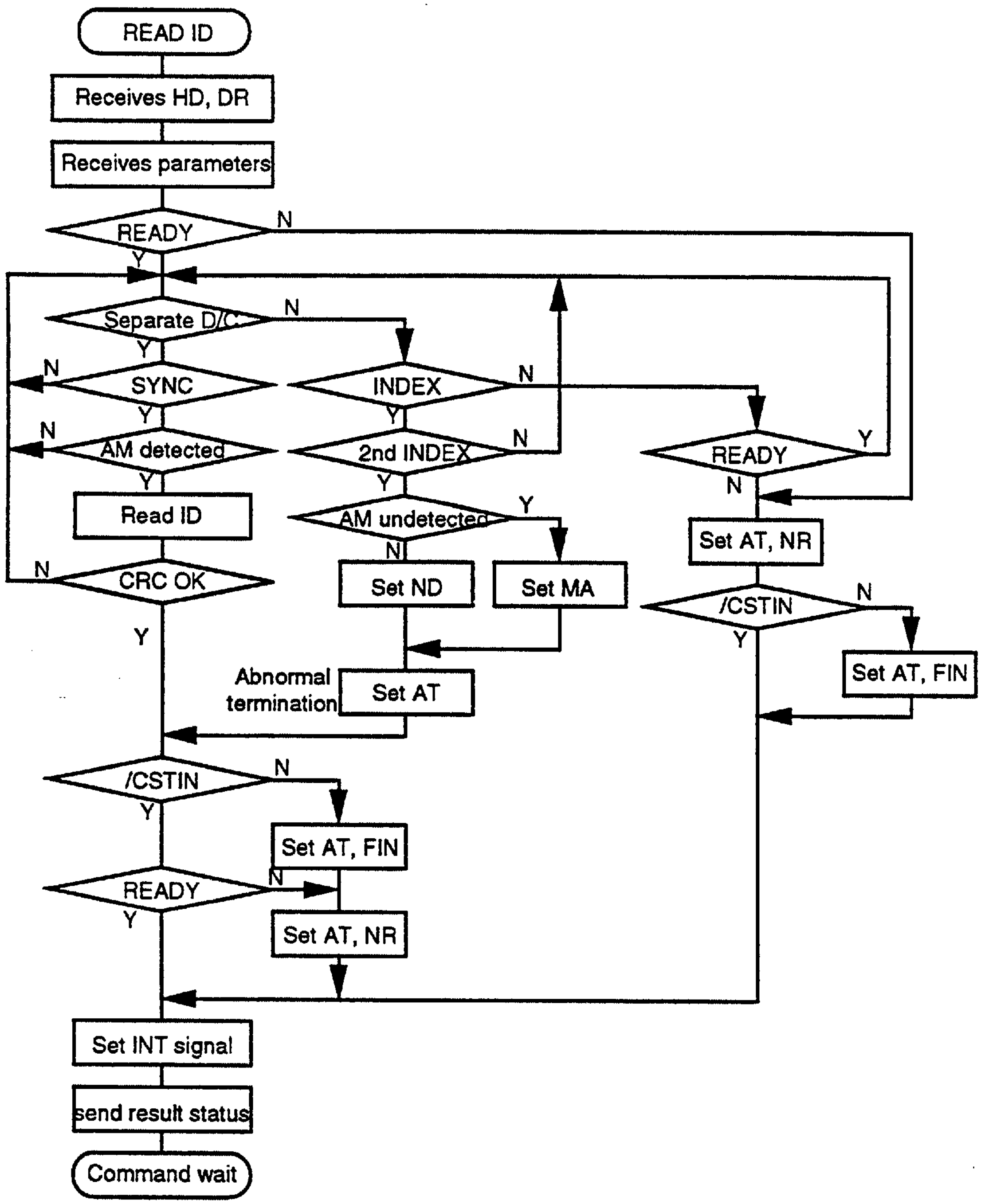
READ DATA (GCR Format)



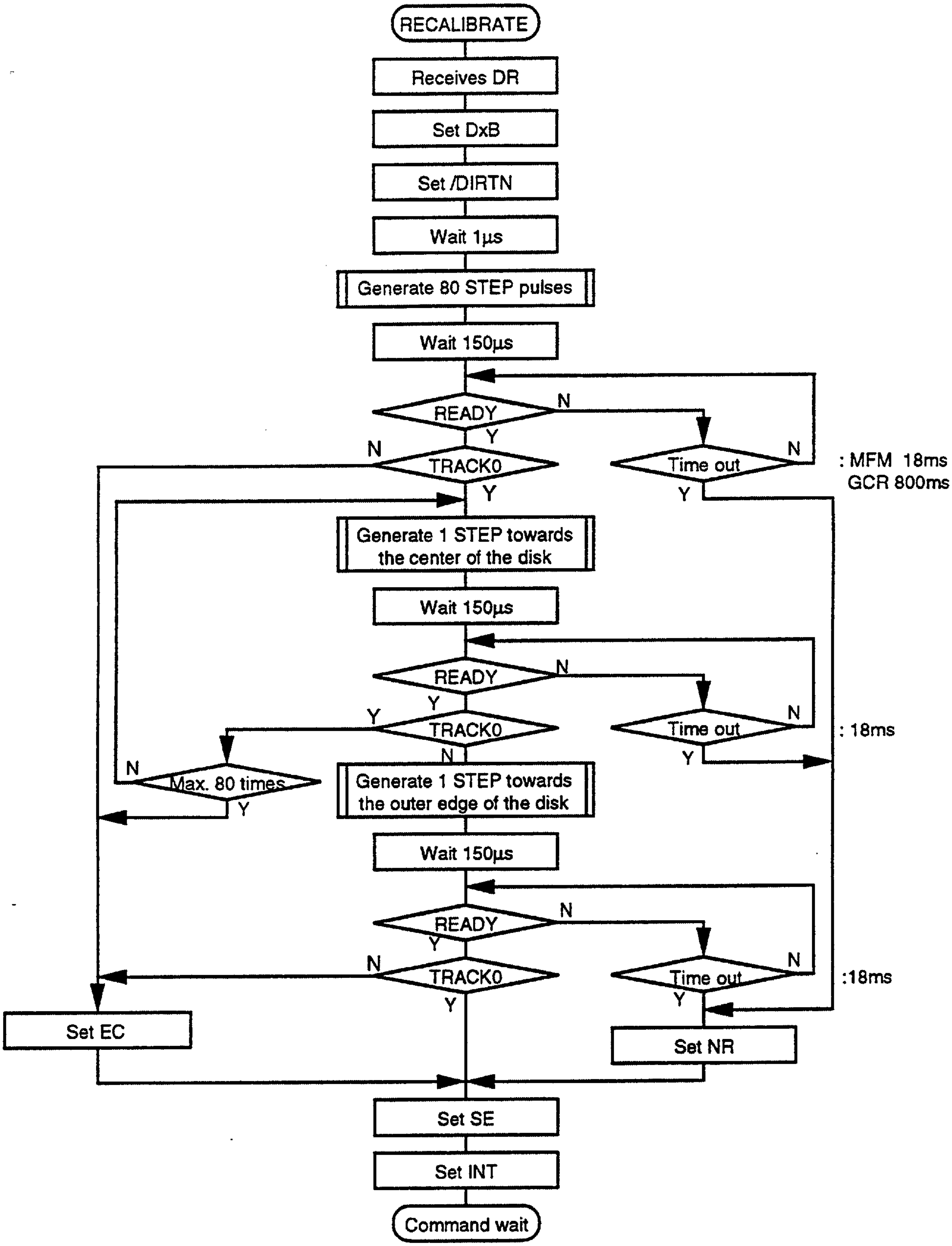
READ DATA (MFM Format)



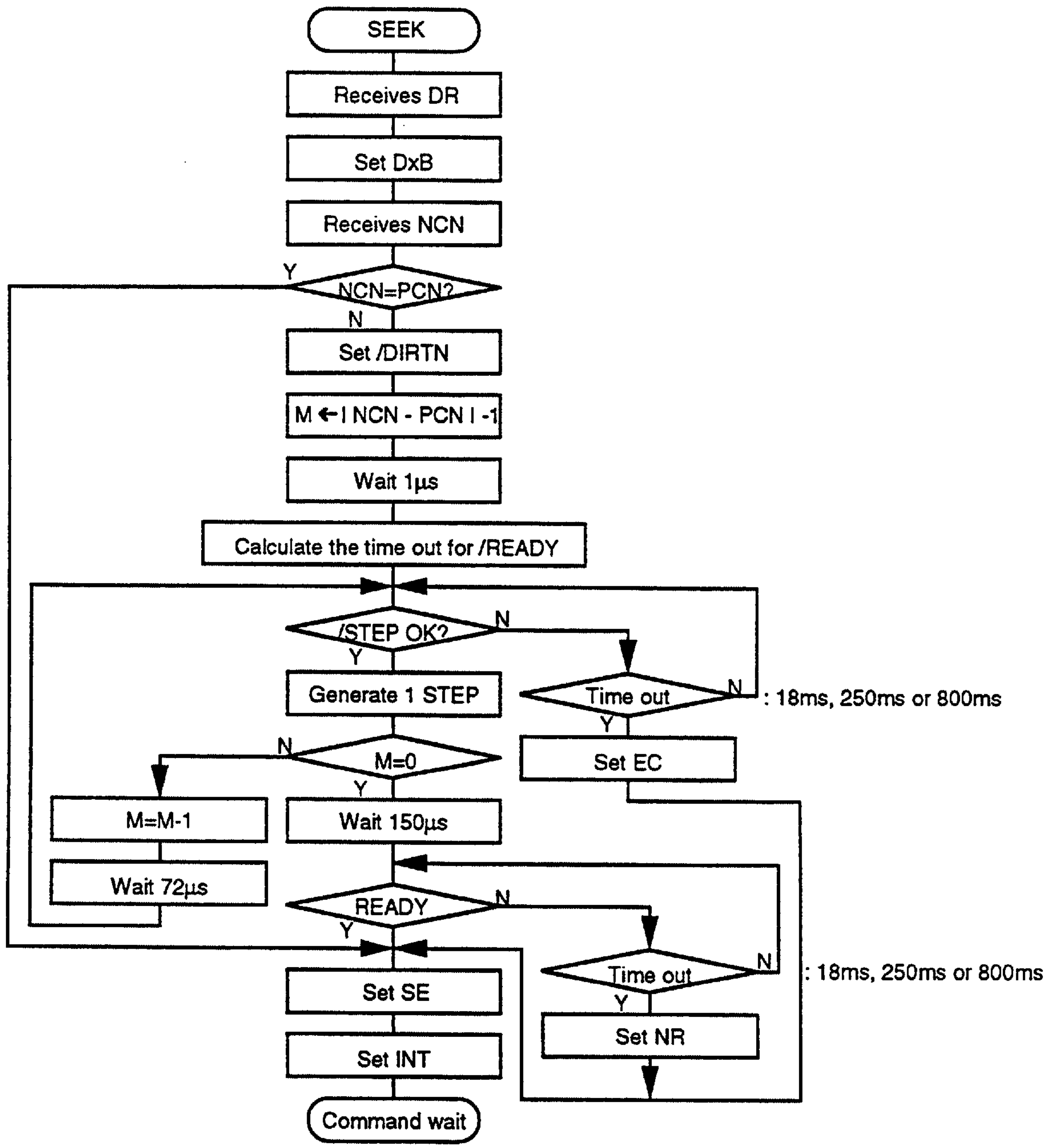
READ ID (MFM Format)



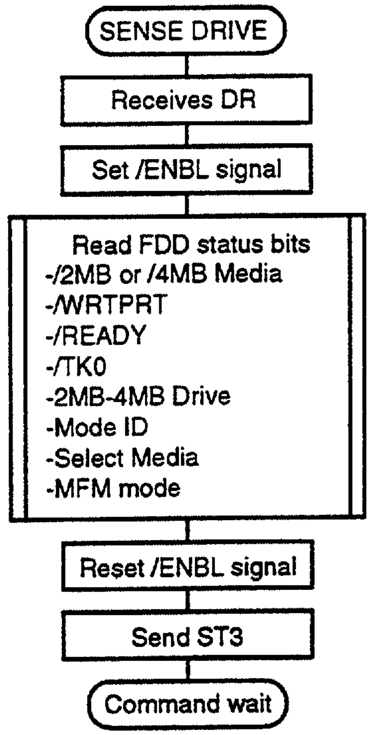
RECALIBRATE



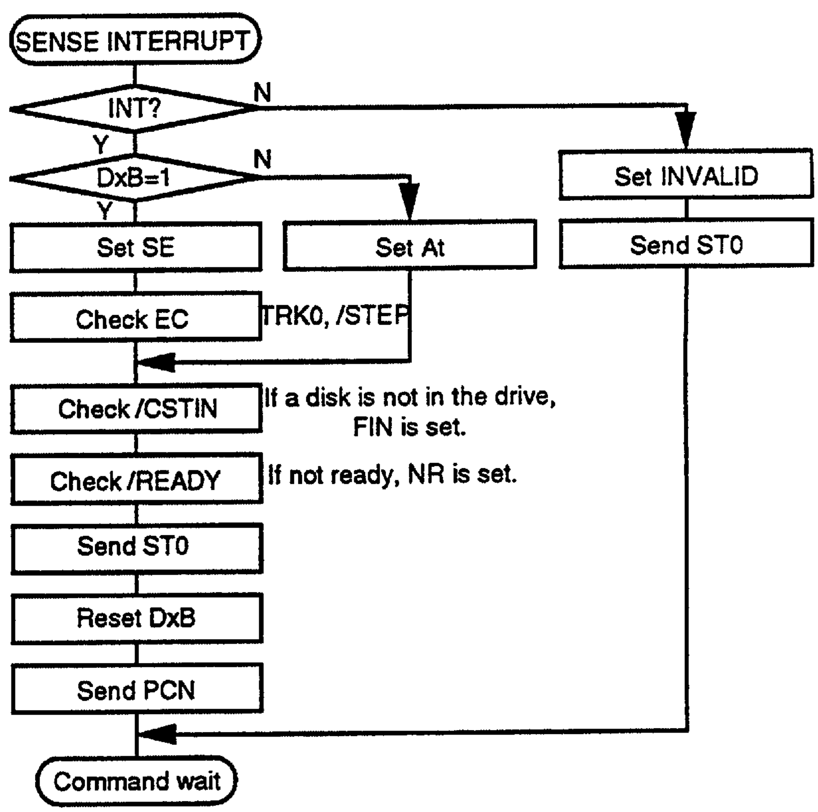
SEEK


SEEK
Receives DR
Set DxB
Receives NCN
NCN=PCN?
Y
N
Set /DIRTN
M ← | NCN - PCN | -1
Wait 1μs
Calculate the time out for /READY
/STEP OK?
N
Y
Generate 1 STEP
Time out
N
: 18ms, 250ms or 800ms
Y
Set EC
M=0
N
Y
M=M-1
Wait 150μs
Wait 72μs
READY
N
Y
Time out
N
: 18ms, 250ms or 800ms
Y
Set SE
Set NR
Set INT
Command wait

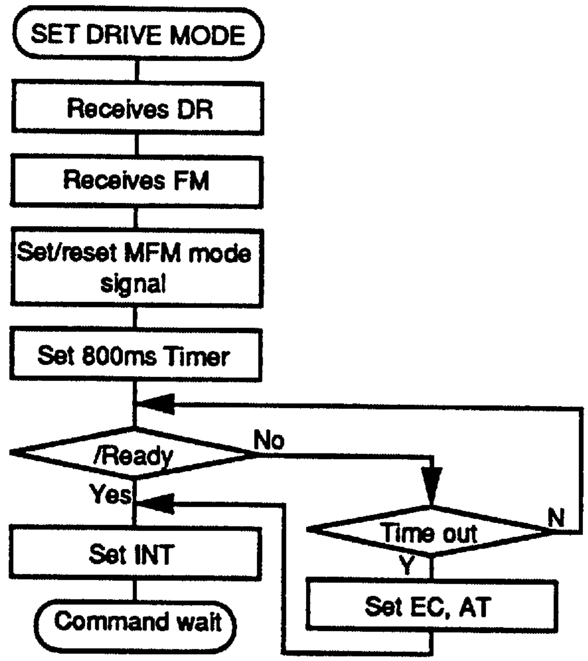
SENSE DRIVE STATUS



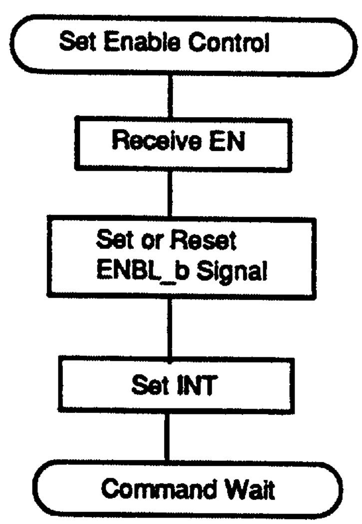
SENSE INTERRUPT STATUS



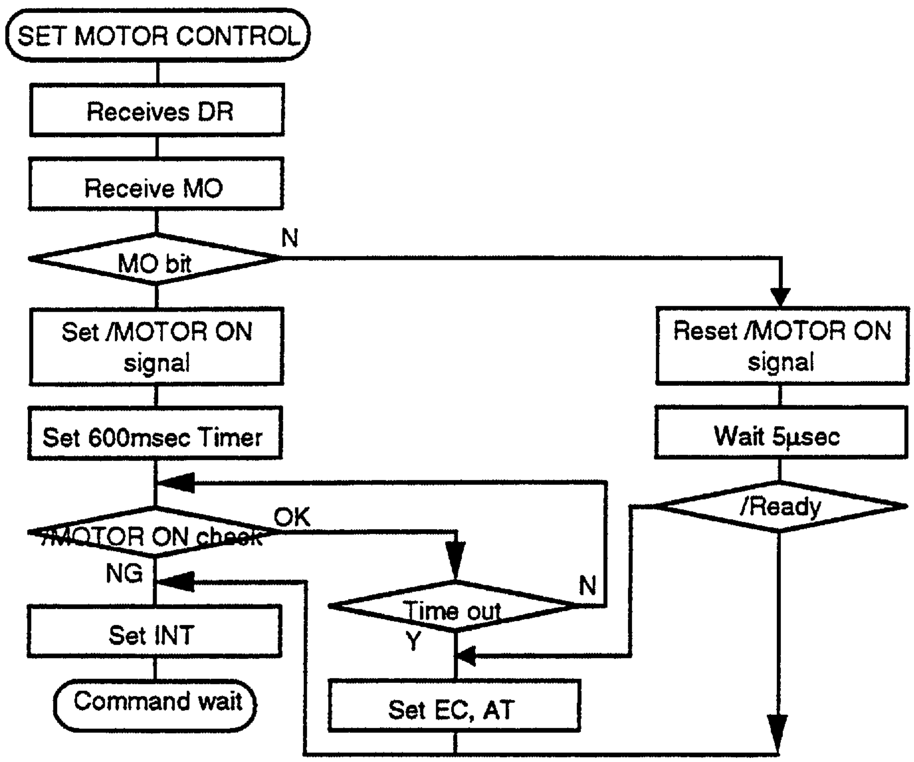
SET DRIVE MODE



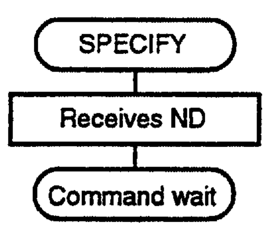
SET ENABLE



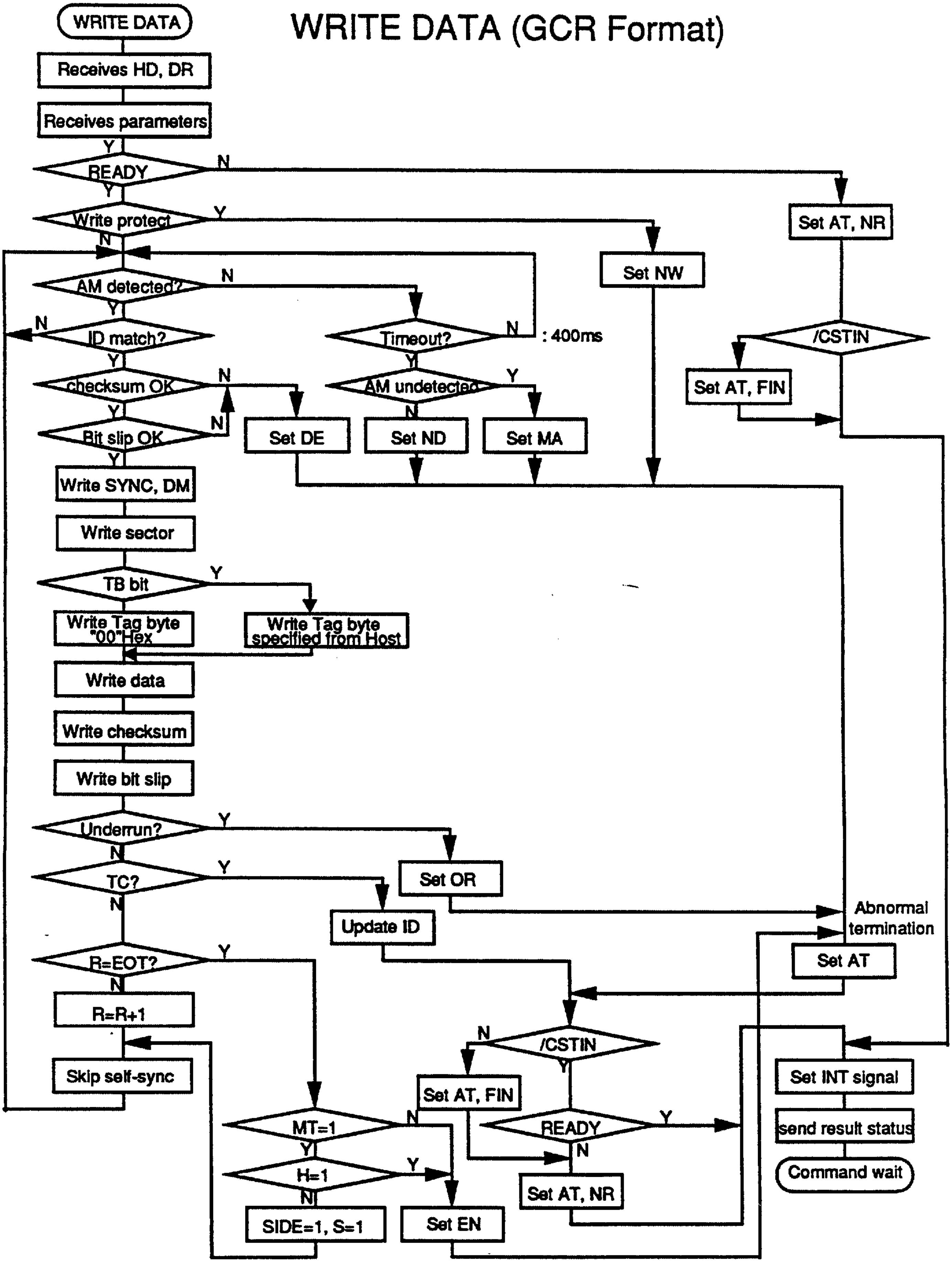
SET MOTOR CONTROL



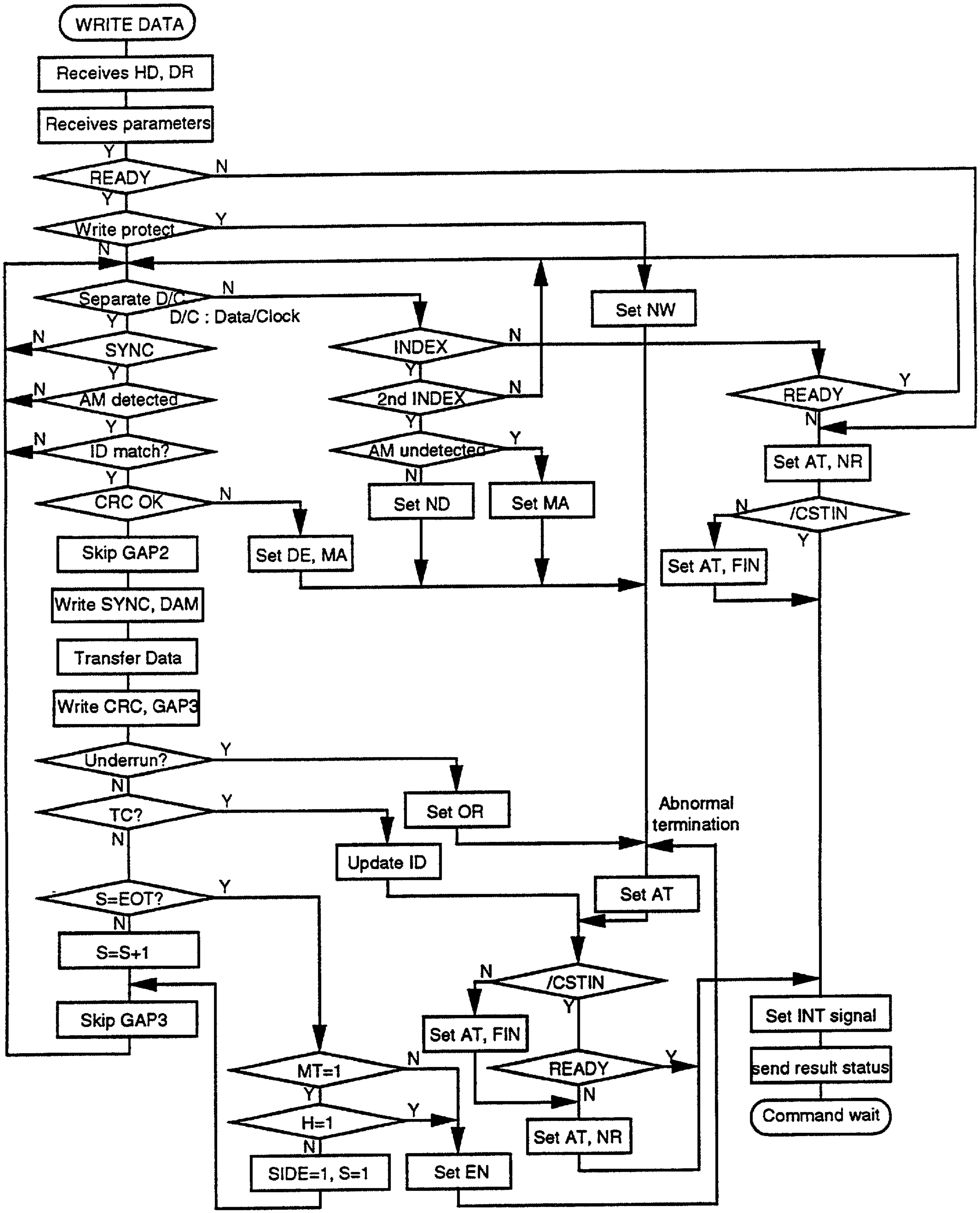
SPECIFY



WRITE DATA (GCR Format)



WRITE DATA (MFM Format)



Chapter 7 DC / AC Specification

Absolute Maximum Ratings

$T_A = +25\ ^oC$

Supply voltage, V_{DD}	-0.5 to +7.0 V
Voltage on any pin (except V_{DD})	-0.5 to V_{DD}+0.5 V
Operating temperature, T_{OPT}	-10 to +70 ^oC
Storage temperature, T_{STG}	-65 to +150 ^oC

Capacitance

$T_A = +25\ ^oC$; V_{DD} = 0V ; f = 1 MHz

Parameter	Symbol	Min	Max	Unit	Conditions
Clock capacitance	C_ϕ		20	pF	Unmeasured pins returned to 0 V
Input capacitance	C_{IN}		20	pF	
Output capacitance	C_{OUT}		20	pF	

DC Characteristics

T_A = -10 to + 70 °C ; V_{DD} = +5V ± 10%

Parameter	Symbol	Min	Max	Unit	Conditions
Low-level input voltage	V_{IL}	-0.5	0.8	V	Except XA1
	V_{IL1}	-0.5	$0.2V_{DD}$	V	XA1
High-level input voltage	V_{IH}	2.2	V_{DD}+0.5	V	Except XA1
	V_{IH1}	0.8VDD	V_{DD}+0.5	V	XA1
Low-level output voltage	V_{OL}		0.45	V	I_{OL} = 12 mA D0-D7,DMARQ,INT, TDO
	V_{OL1}		0.45	V	I_{OL} = 48 mA All other outputs
High-level output voltage (Note1)	V_{OH}	3.0	V_{DD}	V	I_{OH} = - 4.0mA D0-D7,DMARQ,INT, TDO
Input leakage current	I_{IL}		+10	µA	V_{IN} = V_{DD}
			- 10	µA	V_{IN} = 0 V
Output leakage current	I_{OL}		+ 10	µA	V_{OUT} = V_{DD}, Host I/F
			- 10	µA	V_{OUT} = 0.45 V ,Host I/F
			+ 100	µA	V_{OUT} = V_{DD}, FDD I/F
			- 100	µA	V_{OUT} = 0.45 V ,FDD I/F
V_{DD} supply current	I_{DD}		40	mA	
Standby current	I_{DDS}		100	µA	

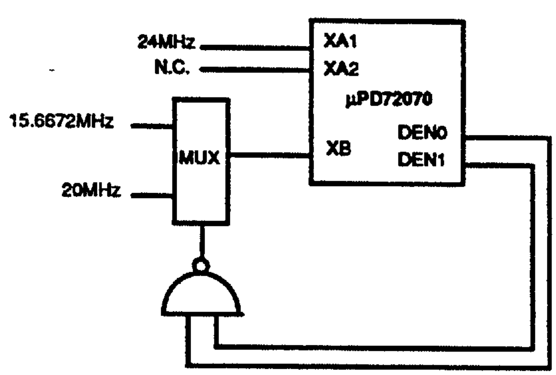
Note 1 : All of FDD interface outputs are Open Drain outputs. In PC/AT™ Mode , DMARQ and INT outputs become Open Drain outputs.

Clock Specifications

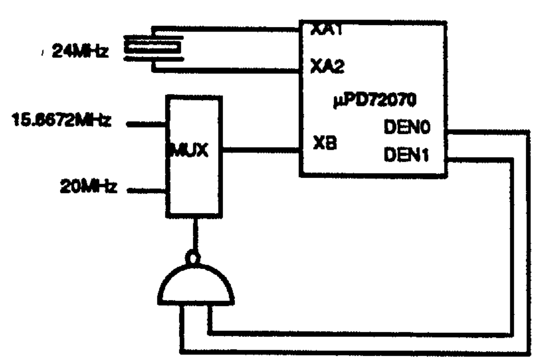
T_A = -10 to + 70 °C ; V_{DD} = +5V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Crystal Resonator Source						
Clock cycle	t_{CYA}		41.66 (24 MHz)		ns	XA1,XA2
Clock cycle permitted				± 0.5	%	
Oscillator stabilization time	t_{KS}	10			ms	
External Clock Fig.1						
Clock cycle	t_{CYA}	41.46	41.66 (24 MHz)	41.87	ns	XA1 pin.
	t_{CYB}	63.42	63.82 (15.6672 MHz)	64.42	ns	XB pin. For GCR FDD
		49.75	50.00 (20 MHz)	50.25	ns	XB pin. For 13Mbyte FDD
Clock high-level width	t_{KKH}	12			ns	
Clock low-level width	t_{KKL}	12			ns	
Clock rise time	t_{KR}			10	ns	
Clock fall time	t_{KF}			10	ns	

Recommended Circuit #1 Crystal Clock Oscillators



Recommended Circuit #2 Crystal Resonator



AC Characteristics

T_A = -10 to + 70 °C ; V_{DD} = +5V ± 10%

Parameter	Symbol	Min	Max	Unit	Conditions
Host Read Timing Fig.2					
A0-A2,CS_b,DMAAK_b setup to RD_b active	t_{AR}	5		ns	
A0-A2,CS_b,DMAAK_b hold from RD_b inactive	t_{RA}	5		ns	
RD_b active pulse width	t_{RR}	50		ns	
DATA valid from RD_b active	t_{RD}		40	ns	
DATA float delay from RD_b inactive	t_{DF}		50	ns	
DATA hold from RD_b inactive	t_{RDH}	5		ns	
RD_b inactive pulse width	t_{RH}	50		ns	
INT delay from RD_b inactive	t_{RI}		50	ns	
Host Write Timing Fig.3					
A0-A2,CS_b,DMAAK_b setup to WR_b active	t_{AW}	5		ns	
A0-A2,CS_b,DMAAK_b hold from WR_b inactive	t_{WA}	5		ns	
WR_b active pulse width	t_{WW}	50		ns	
DATA setup to WR_b inactive	t_{DW}	50		ns	
DATA hold from WR_b inactive	t_{WD}	5		ns	
WR_b inactive pulse width	t_{WH}	50		ns	
INT delay from WR_b inactive	t_{WI}		50	ns	

Parameter	Symbol	Min	Max	Unit	Conditions
DMA Timing Fig.4					
DMARQ cycle period	t_{MCY}	8 / DTR		µs	Note 1
DMAAK_b active to DMARQ inactive	t_{AM}		50	ns	
RD_b / WR_b active to DMARQ inactive	t_{RWM}		50	ns	
DMAAK_b setup to RD_b / WR_b active	t_{ARW}	5		ns	
DMAAK_b hold from RD_b / WR_b inactive	t_{RWA}	5		ns	
DMARQ active to RD_b / WR_b active	t_{MRWA}	0		ns	
TC pulse width	t_{TC}	50		ns	
TC active to DMARQ inactive	t_{TM}		50	ns	
DMAAK_b active pulse width	t_{AA}	50		ns	
DMAAK_b inactive pulse width	t_{AI}	50		ns	
DMARQ active to DMAAK_b active	t_{MA}	0		ns	
DMARQ active to RD_b / WR_b inactive	t_{MRW}		6.5 / DTR	µs	Note 2
DMARQ active to TC active	t_{MT}		6.5 / DTR	µs	Note 2
Reset Timing Fig.5					
RESET pulse width	t_{RST}		170	t_{CYA}	Note3
RESET to control inactive	t_{RC}		2	µs	

Note1 : DTR means Data Transfer Rate.For example ,when Data Transfer Rate is 500Kbps,DMARQ cycle period is as follows.

$$t_{AW} = 8 / DTR = 8 / 500\,000 = 16\,\mu s$$

Note2 : DTR means Data Transfer Rate.This value , 6.5 / DTR , appear Over-Run error timing with the FIFO disabled. When the FIFO enabled , add (FIFO-threshold x 8 / DTR) to the this value.

Note3 : This value include Hardware Reset pulse width , waiting term after the SOFTWARE RESET command wrote and waiting term the FDCRST_b bit of Digital Output Register (DOR) activated.

Parameter	Symbol	Min	Max	Unit	Conditions
MFM FDD Write Data Timing Fig.6					
WDATA_b pulse width	t_{WDD}	0.125/DTR		s	Note1
SIDE_b setup to WGATE_B active	t_{SDWG}	100		µs	
SIDE_b hold from WGATE_b inactive	t_{WGSD}	750		µs	
MFM FDD Read Data Timing Fig.7					
RDATA_b pulse width	t_{RDD}	50		ns	
RDATA_b cycle period	t_{RDCY}		800	ns	1.25Mbit / sec
MFM FDD Control Timing Fig.8					
DIR_b setup to STEP_B active	t_{DST}	0.5/DTR		s	
DIR_b hold from STEP_B inactive	t_{STD}	12/DTR		s	
STEP_b pulse width	t_{STP}	3/DTR		s	
STEP_b cycle period	t_{SC}	500/DTR		s	Note2
INDEX_b pulse width	t_{IDX}	100		ns	

Note1 : DTR means Data Transfer Rate.For example ,when Data Transfer Rate is 500Kbps,WDATA pulse width is as follows.

t_{WDD} = 0.125/DTR = 0.125 / 500 000 = 250 ns

Note2 : DTR means Data Transfer Rate.For example ,when Data Transfer Rate is 500Kbps, Step pulse width is as follows.

t_{sc} = 500/DTR = 500 / 500 000 = 1ms

Fig.1 External Clock

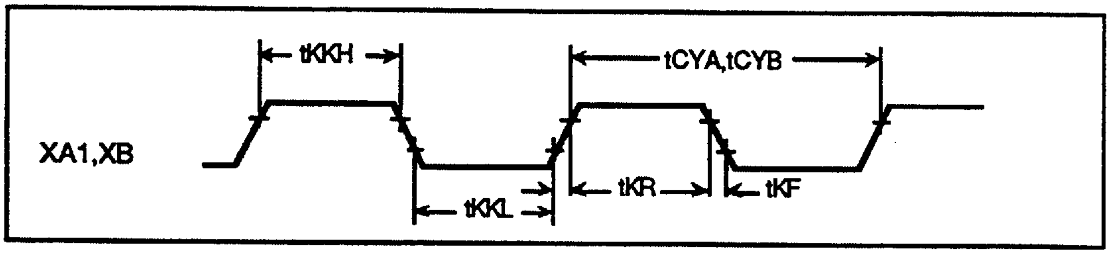


Fig.2 Host Read Timing

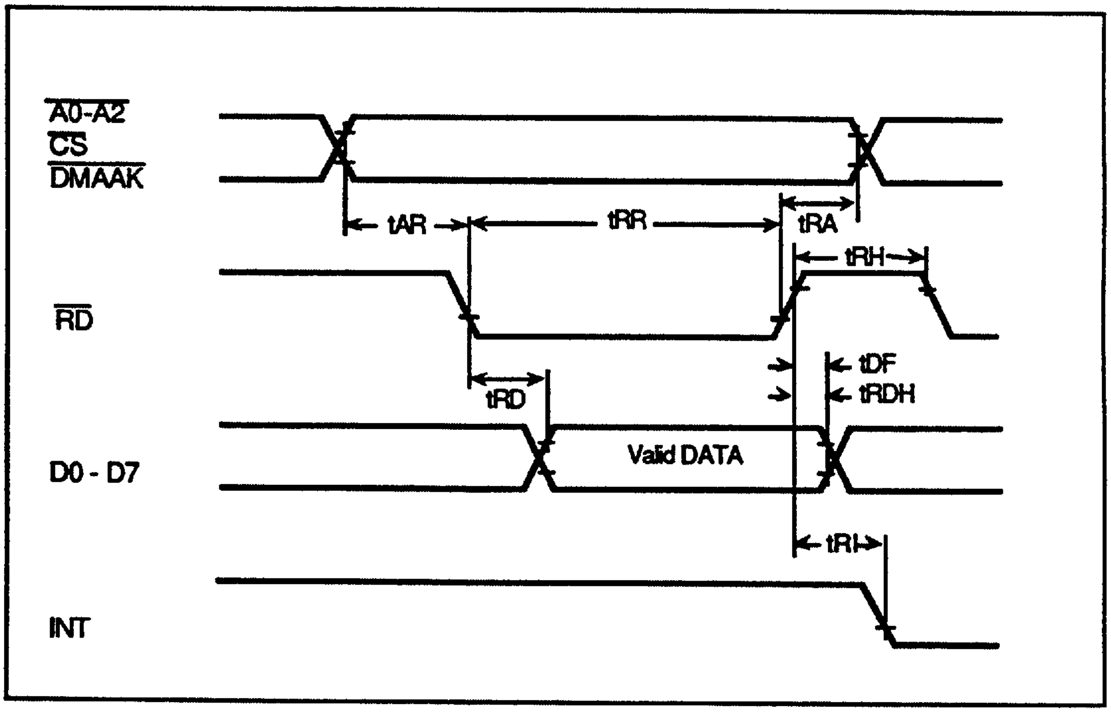


Fig.3 Host Write Timing

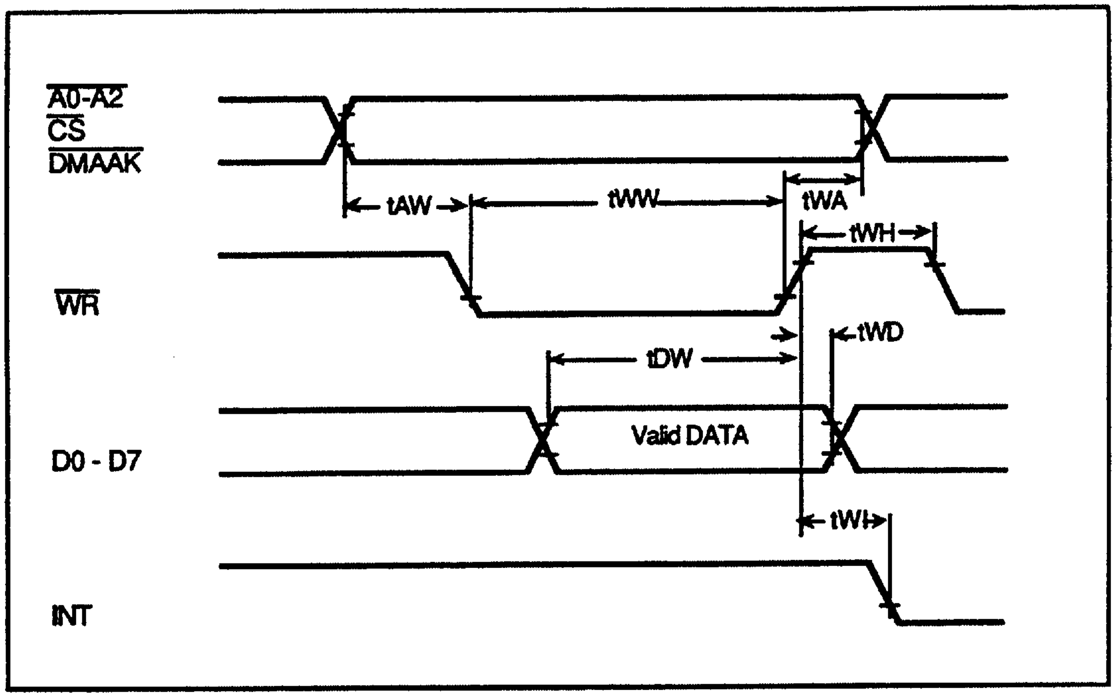


Fig.4 DMA Timing

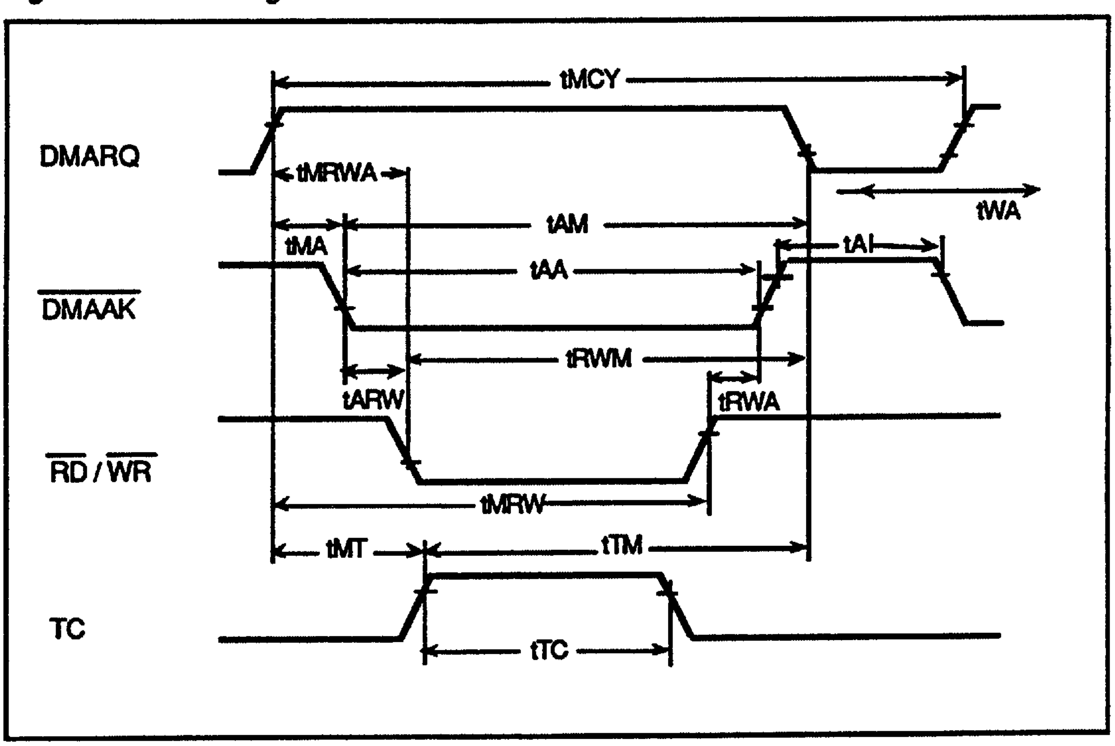


Fig.5 Reset Timing

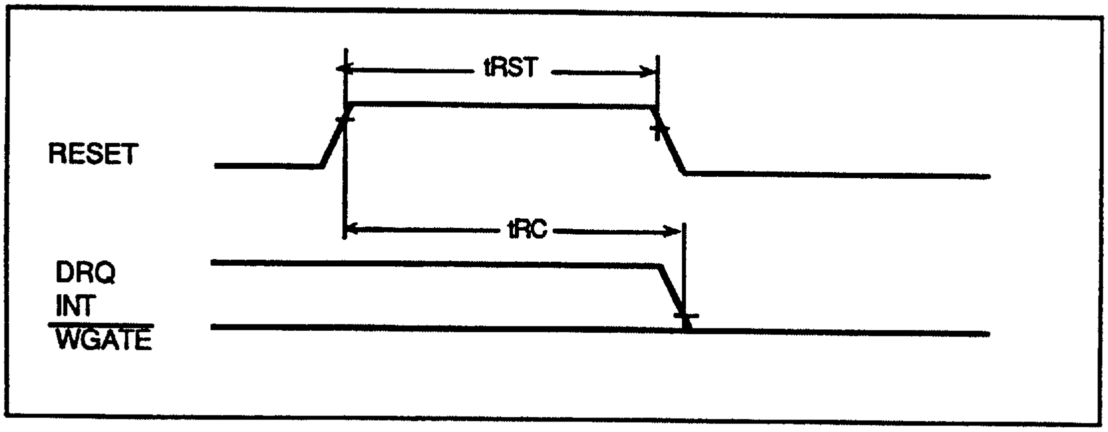


Fig.6 MFM FDD Write Data Timing

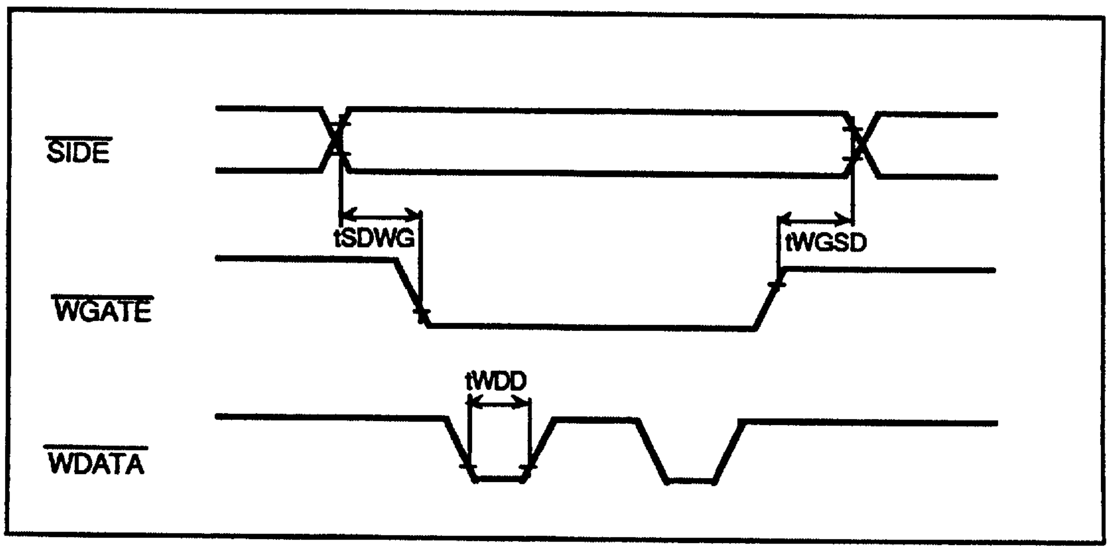
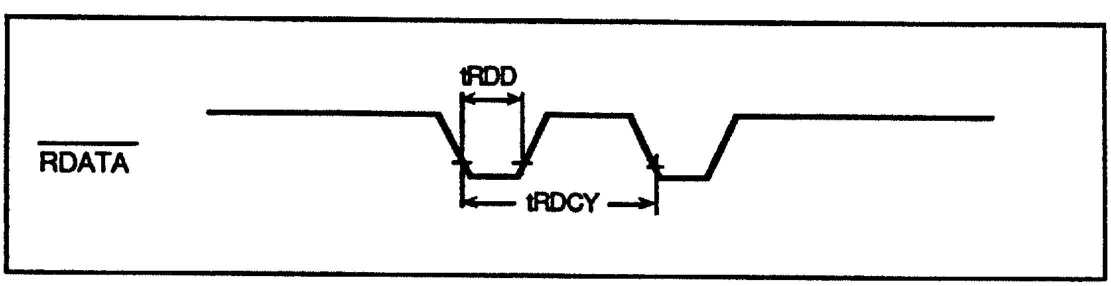


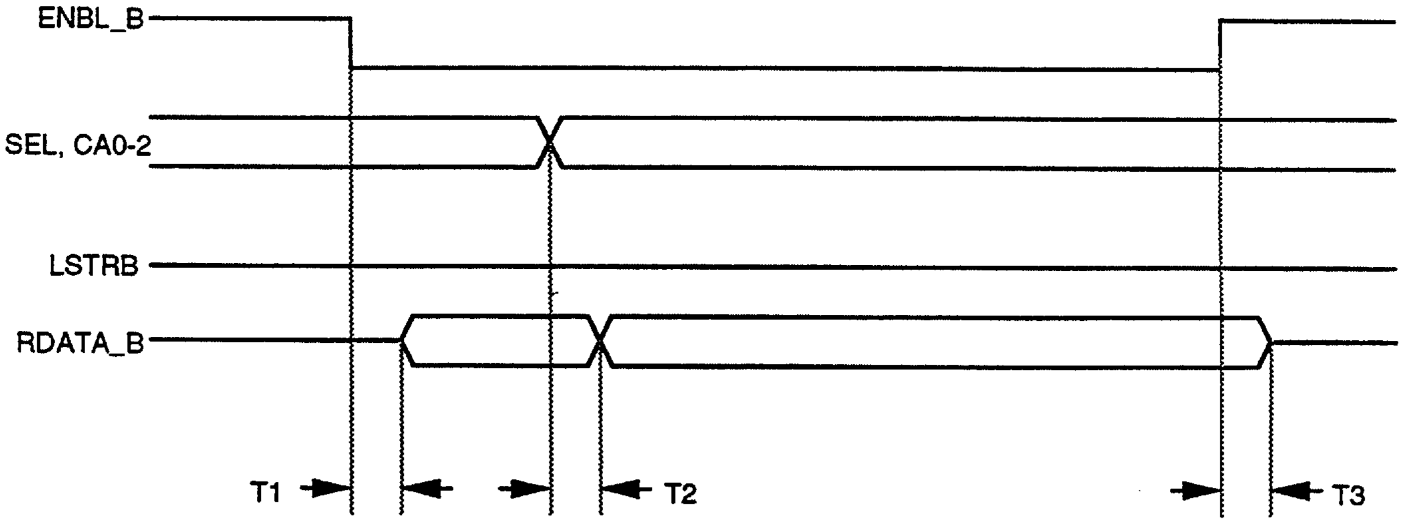
Fig.7 MFM FDD Read Data Timing



7.1 AC Timing Diagrams for the Apple Disk Interface

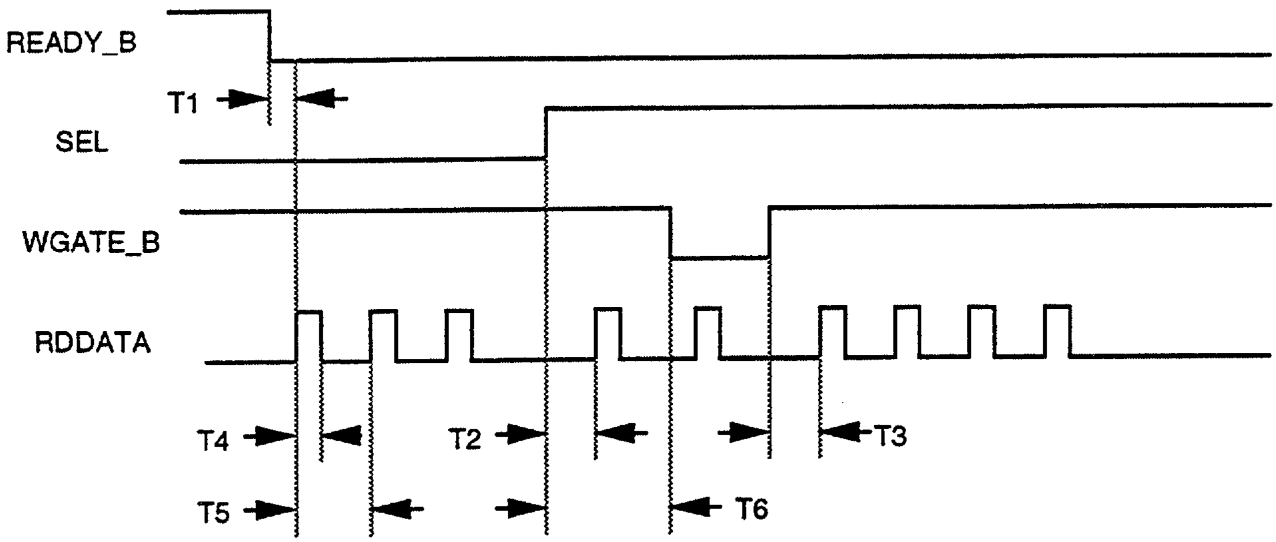
READING DRIVE STATUS

The following timing applies to /DIRTIN, /STEP, /MOTOR ON, EJECT, 2MB DRIVE, 4MB DRIVE, Mode ID, RDDATA, /DRVIN, /TACH, or INDEX, /READY, /CSTIN, /WRTPRT, /TK0, /2MB MEDIA, /4MB MEDIA, MFM MODE.



T1: 0.5µs max
T2: 0.5µs max
T3: 0.5µs max for high impedance state

READING RDATA



GCR mode

T1: 0.5µsec max
T2: 100µsec max
T3: 190µsec max
T4: 0.15µsec min, 0.8µsec max
T5: 2,4,6µsec nomal
T6: 100µsec min

MFM, 1MB mode

T1: 0.5µsec max
T2: 100µsec max
T3: 190µsec max
T4: 0.15µsec min, 0.8µsec max
T5: 2,3,4µsec normal
T6: 100µsec min

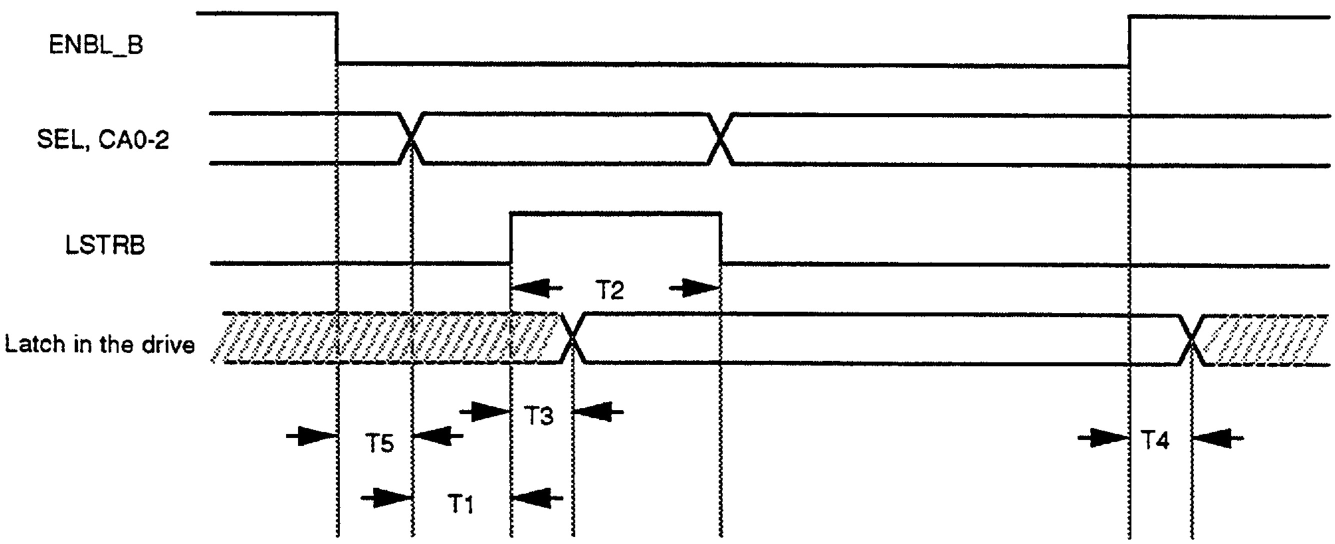
MFM, 2MB mode

T1: 0.5µsec max
T2: 100µsec max
T3: 340µsec max
T4: 0.15µsec min, 0.8µsec max
T5: 2,3,4µsec normal
T6: 100µsec min

MFM, 4MB mode

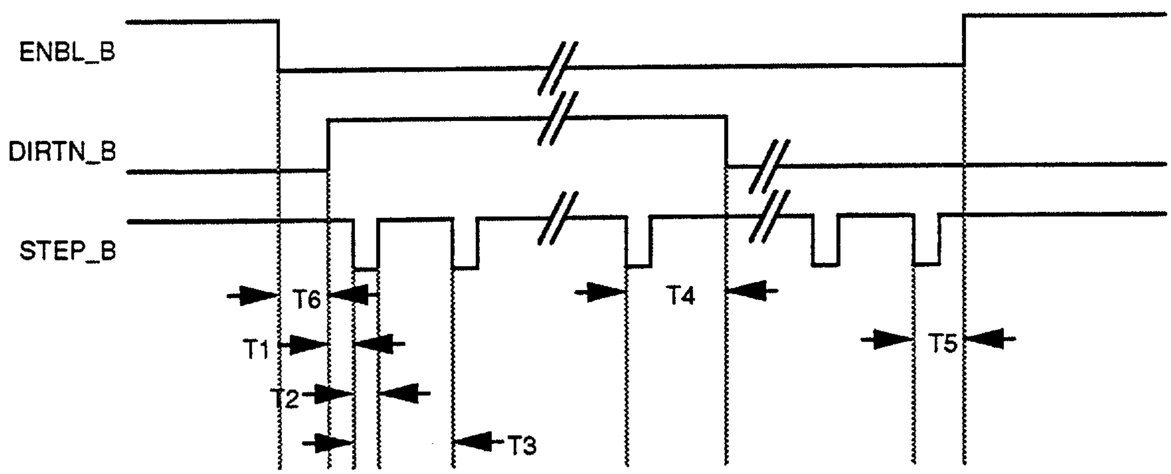
T1: 0.5µsec max
T2: 100µsec max
T3: 340µsec max
T4: 0.15µsec min, 0.8µsec max
T5: 1,1.5,2µsec normal
T6: 100µsec min

SENDING A CONTROL COMMAND



T1: 0.5µsec min
T2: 1.0µsec min
T3: 1.0µsec max
T4: 0.5µsec max
T5: 0.5µsec min

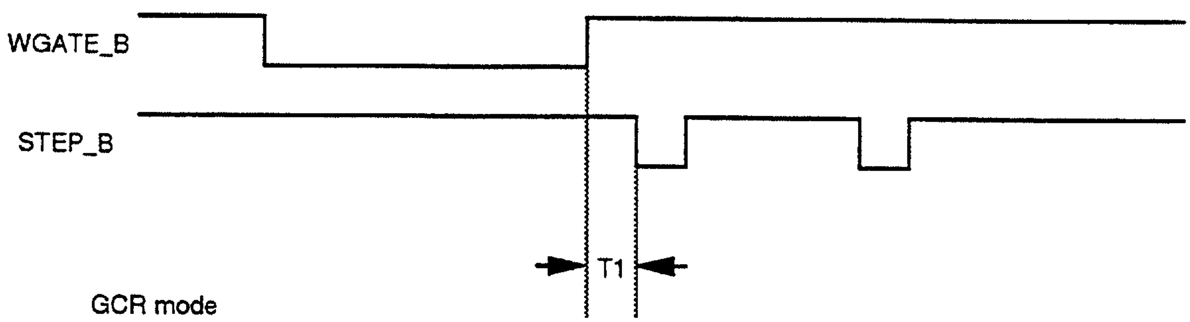
/STEP AND /DIRTIN TIMING



T1: 1.0μs min
T2: 0.5μs min
T3: 72μs min
T4: See NOTE
T5: 37μs min
T6: 0.5μs min

NOTE: It is not allowed to change /DIRTN during head movement or head setting.

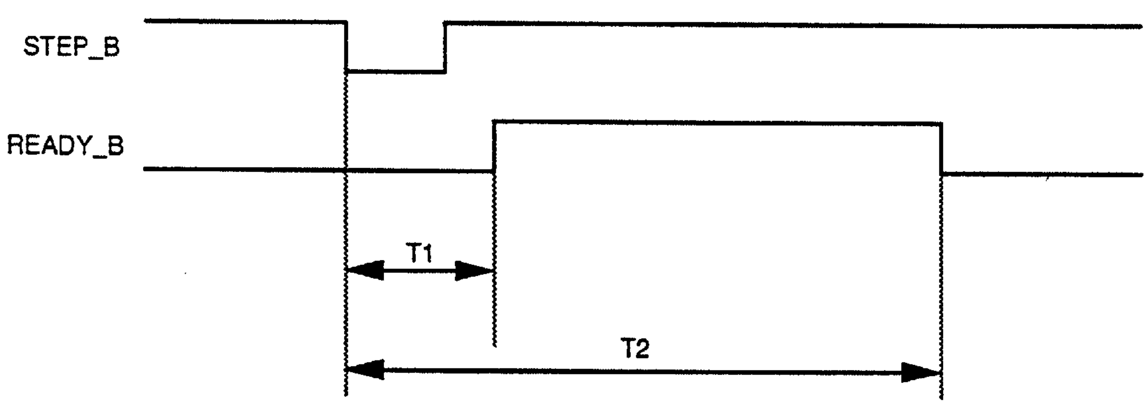
/STEP AND WGATE TIMING



GCR mode
T1: 190µs min

MFM mode
(1MB) T1: 190µsec min
(2MB) T1: 340µsec min
(4MB) T1: 340µsec min

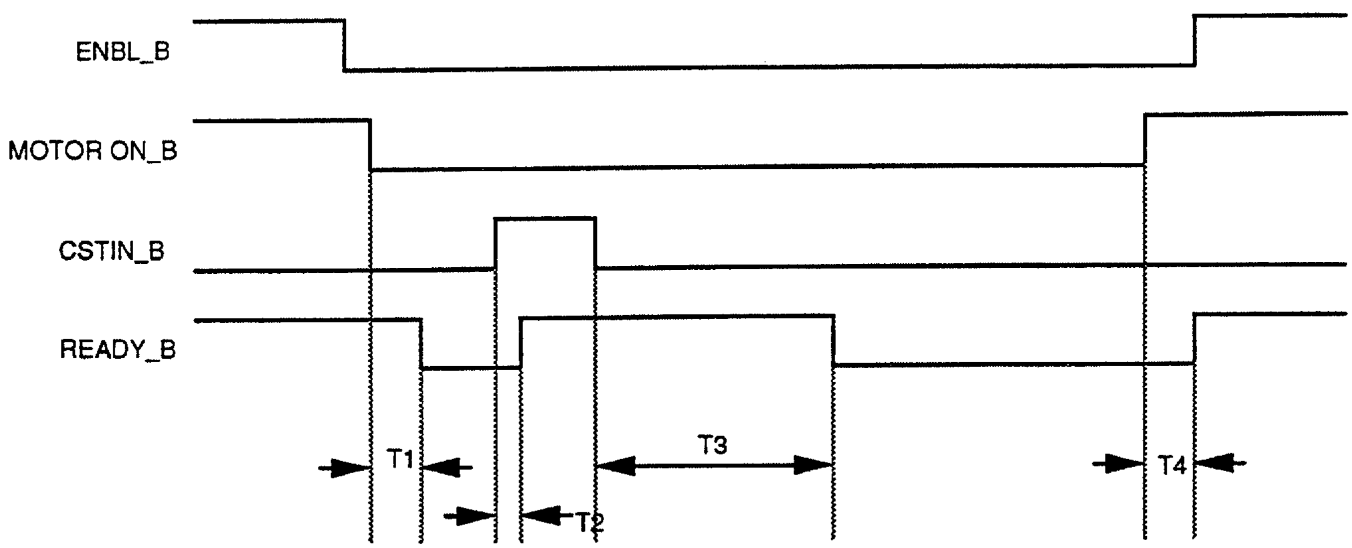
/READY FOR TRACK ACCESS



T1: 150µsec max.

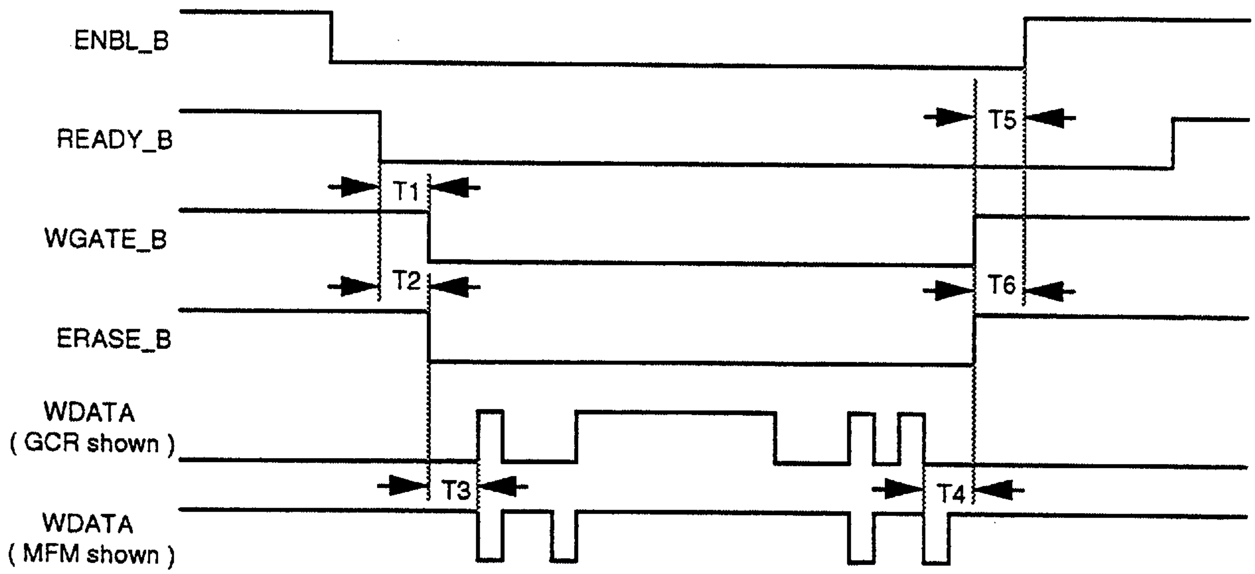
T2: 18msec max. to move one track without speed block change
250msec max. to move one track with speed block change (GCR mode)
800msec max. for any case when step pulses are sent at the maximum rate

/READY FOR MOTOR-ON OR DISK-IN



T1: 600msec max.
T2: 0.5µsec max.
T3: 1.0sec max.
T4: 5µsec max.

/WGATE, WDATA, AND /ERASE TIMING



Note: ERASE_B is a signal internal to the drive.

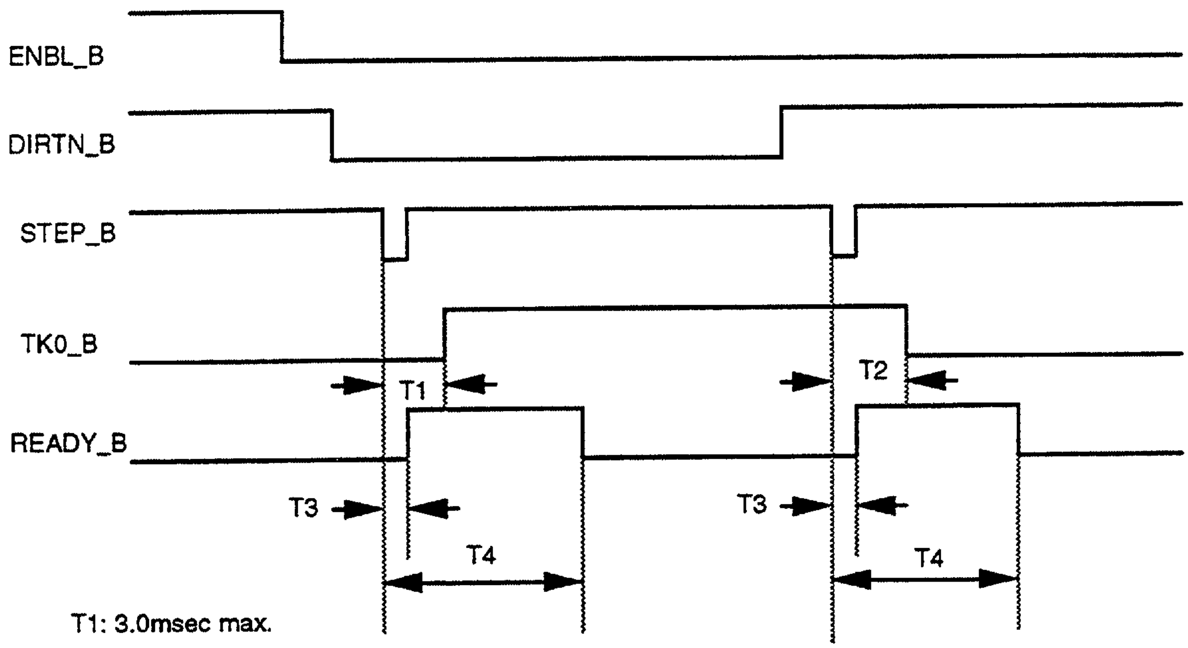
GCR mode

T1: 0.5 μsec min.after stepping
600msec min.after motor on
T2: Same as T1
T3: 1.8μsec min.
T4: 2μsec min.
T5: 0.5 μsec min.
T6: Same as T5

MFM; 1MB, 2MB, and 4MB mode

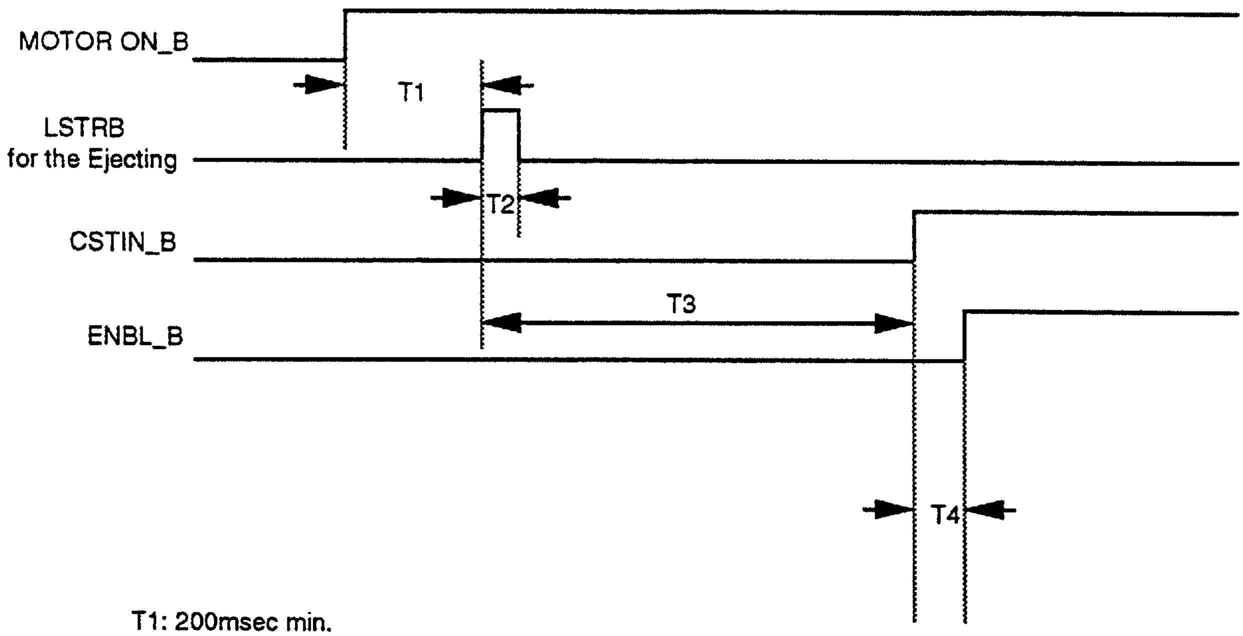
T1: 0.5 μsec min.after stepping
600msec min.after motor on
T2: Same as T1
T3: 4μsec min.
T4: 2μsec min.
T5: 0.5 μsec min.
T6: Same as T5

TK0 TIMING



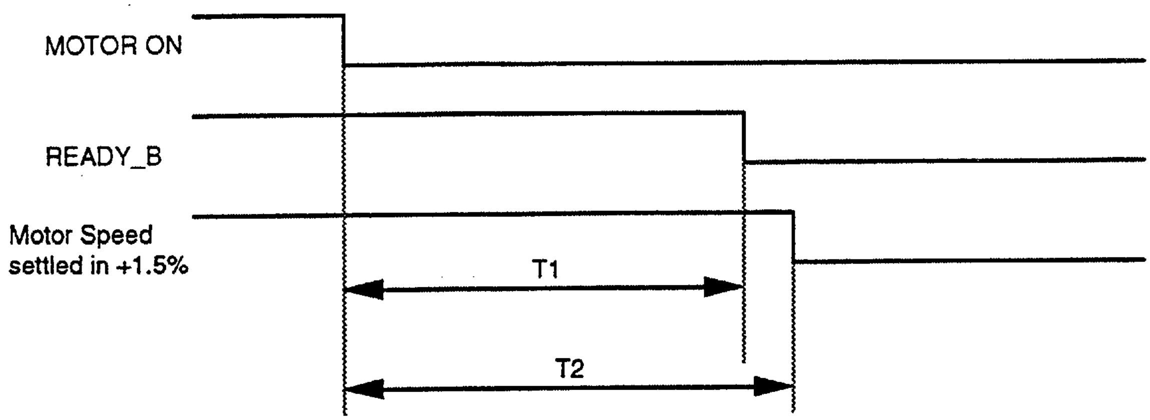
T1: 3.0msec max.
T2: 3.0msec max.
T3: 150μsec max.
T4: 18msec max.

/CSTIN AND /MOTOR ON



T1: 200msec min.
T2: 1.0μsec min.
T3: 1.5sec max.
T4: 150μsec min.

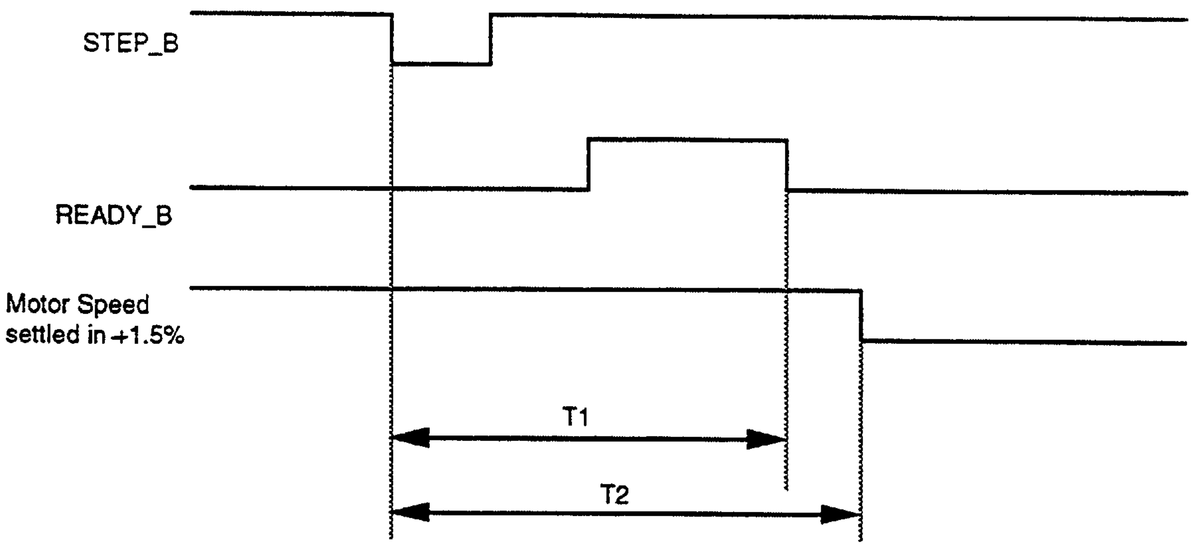
MOTOR START



T1: 600msec max

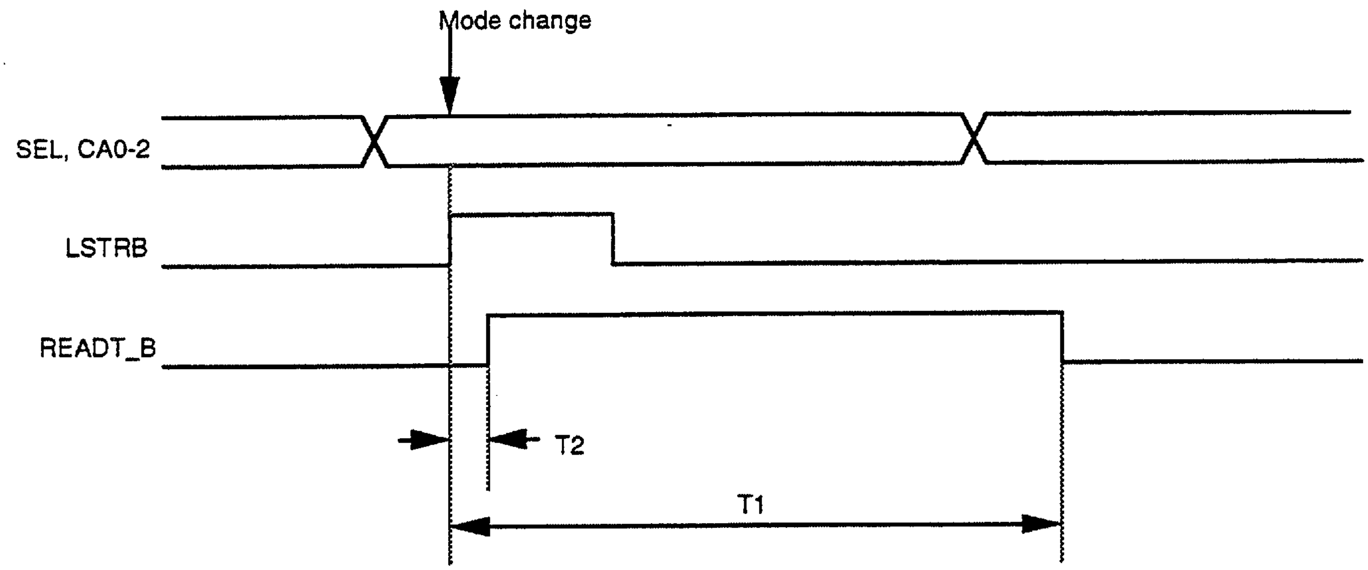
T2: 1sec max

SPEED ZONE BOUNDARY CROSSING, MOTOR SPEED SETTLING TIME



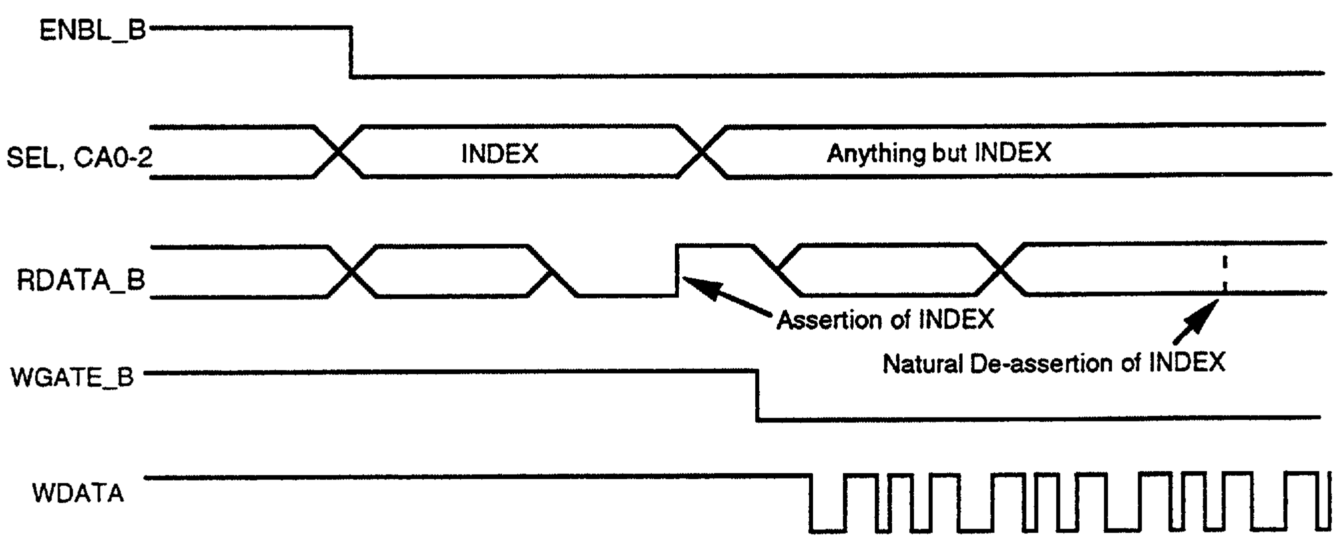
T1: 250msec max.
T2: 250msec max.

/READY FOR MODE CHANGE (MFM TO GCR OR VISE-VERSA)



T1: 800msec max.
T2: 20msec max.

SPECIAL CONDITION FOR INDEX WHEN WRITING DATA



Chapter 8 JTAG Specification

8.1 Features

This JTAG implementation into the FDC has the following features:

1) Compatibility with IEEE1149.1 JTAG Boundary Scan Standard
2) Only three Registers:
   - Instruction
   - Bypass
   - Boundary Scan

(There is no Identification or other Test Data registers in the FDC)

3) Supports the following instructions:
   - Bypass instruction
   - Sample/Preload instruction
   - Extest instruction
   - No support for RUNBIST, Intest and other instructions
4) Special pins for JTAG:
   - TCK
   - TMS
   - TDI
   - TDO

8.2 Block Diagram

Fig. 8.2 shows the block diagram of this implemented JTAG, which is mainly consisted of the TAP controller, the Instruction register, the Instruction decoder, the Bypass register and the Boundary Scan register.

The Instruction register is consisted of the two bits shift registers and the instruction data to be written should be transfered through the TDI pin. The written data as instruction can determine what register should be selected or what a kind of instruction should be operated.

The TAP controller can change its operated state according to the data of the TMS latched at the rising clock of the TCK pin.

The Bypass register is consisted of one shifted register to be connected between the TDI and the TDO pins in the Shift-DR state of the TAP controller and to be shifted toward the TDO pin at each the falling of the TCK pin when this register is selected during the shift-DR state in the TAP. Especially, when this instruction is selected, the operation of this JTAG circuitry does not effect on

the operation of the FDC.

The Boundary Scan register is located between the external pins and the internal logic in the FDC and this register can latch or load data according to the instruction from the TAP controller when this register is selected.

This register is to be shifted toward the TDO pin at each the falling of the TCK pin and to output the LSB (Least Significant Bit) from the TDO pin when this register is selected during the shift-DR state in the TAP. Especially, when this instruction is selected, the operation of this JTAG circuitry does not effect on the operation of the FDC.

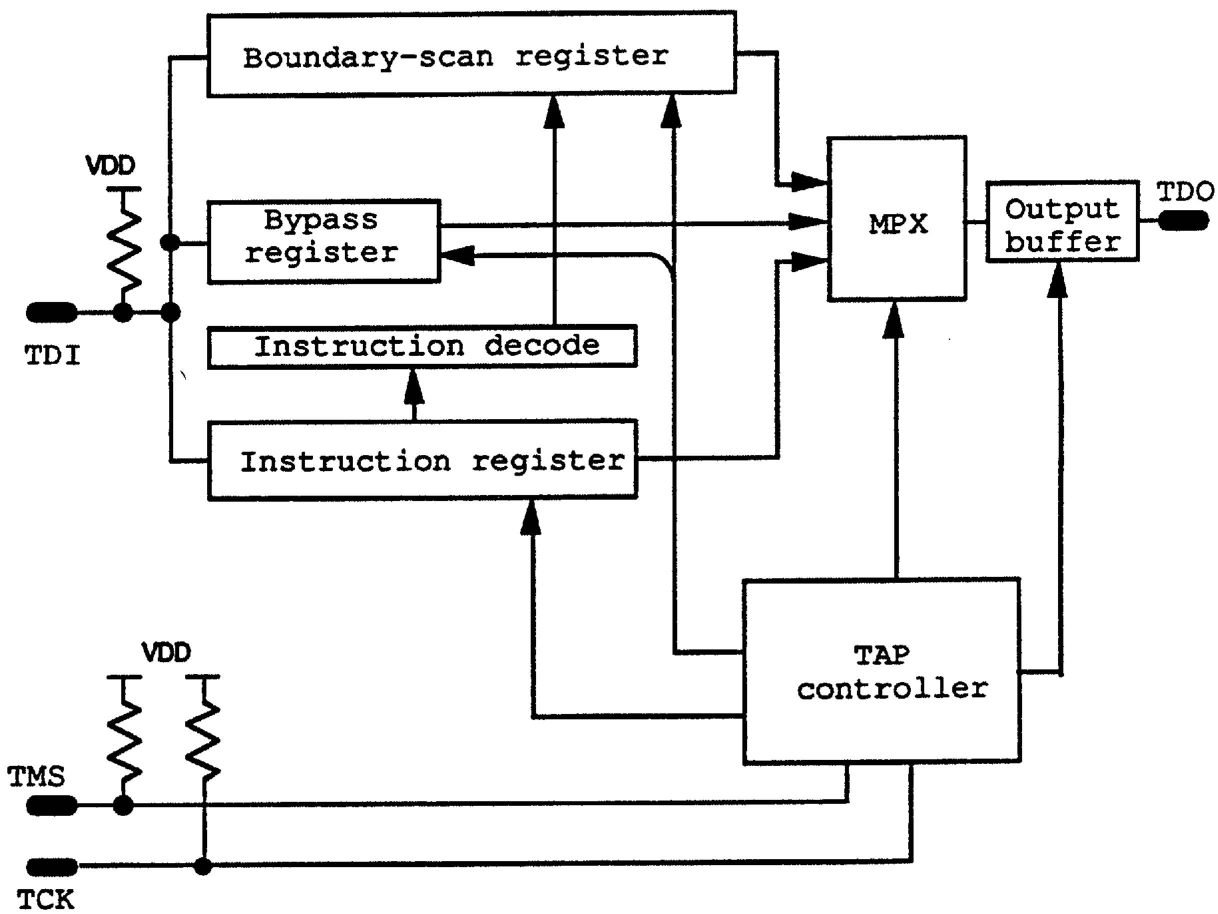


Fig 8.2 A Block Schematic of the Test Logic

8.3 Pin Functions

There are four pins to be needed for this JTAG circuitry; TCK, TMS, TDI and TDO.

The TCK pin can be used to provide the clock signal for only this JTAG circuitry. This clock signal is separated from the FDC system clocks in this

chip.

The TMS pin can be used to define the operated TAP controller according to the value of this pin latched at the rising of the TCK pin. In addition, this pin is internally pulled up by the resistor with approximately from 50k Ohm to 200k Ohm.

The TDI can be used to transfer data into the internal registers implemented in this JTAG circuitry. This pin also internally pulled up by the resistor with approximately from 50k Ohm to 200k Ohm.

The TDO can be used to be provided the output data from internal registers. The output signal is changed at the falling of the TCK pin. In addition, the output of this pin have three states; high, low and high impedance in logical states to be controlled by the TAP controller.

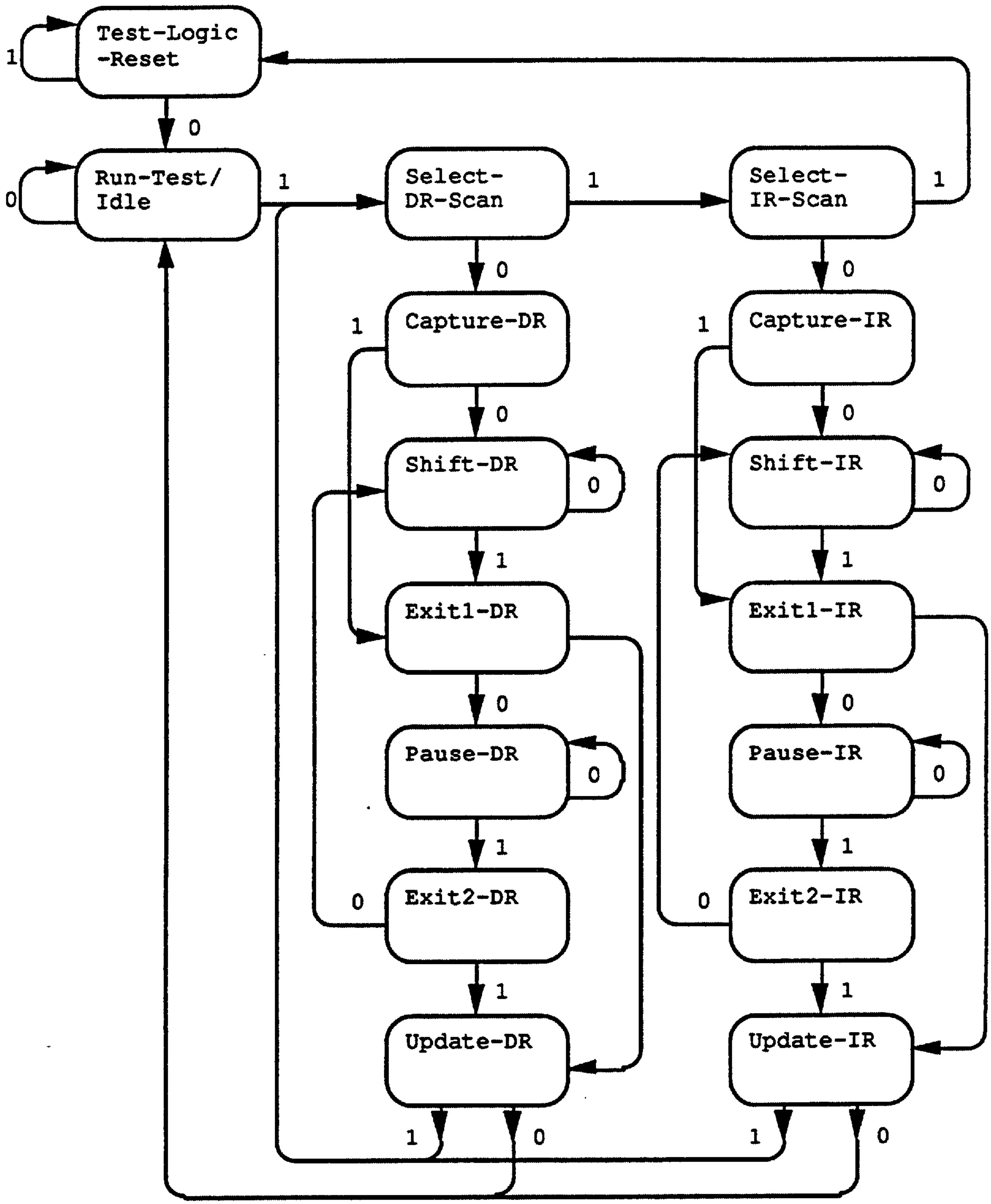
8.4 Operations

8.4.1 TAP Controller

The TAP controller is a synchronous finite state machine that responds to changes at the TMS and TCK signals of the TAP and controls the sequence of operations of the circuitry defined by the IEEE standard 1149.1.

8.4.1.1 TAP Controller State Diagram

The state diagram for the TAP controller is as shown in Fig 8.4.-1. All state transitions of the TAP controller occurs based on the value of TMS at the time of a rising edge of TCK. Actions of Instruction, Boundary-Scan and Bypass registers occur on either the rising or the falling edge of TCK in each controller state as shown by Fig 8.4.-2.



NOTE: The value shown adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.

Fig 8.4-1 TAP Controller State Diagram

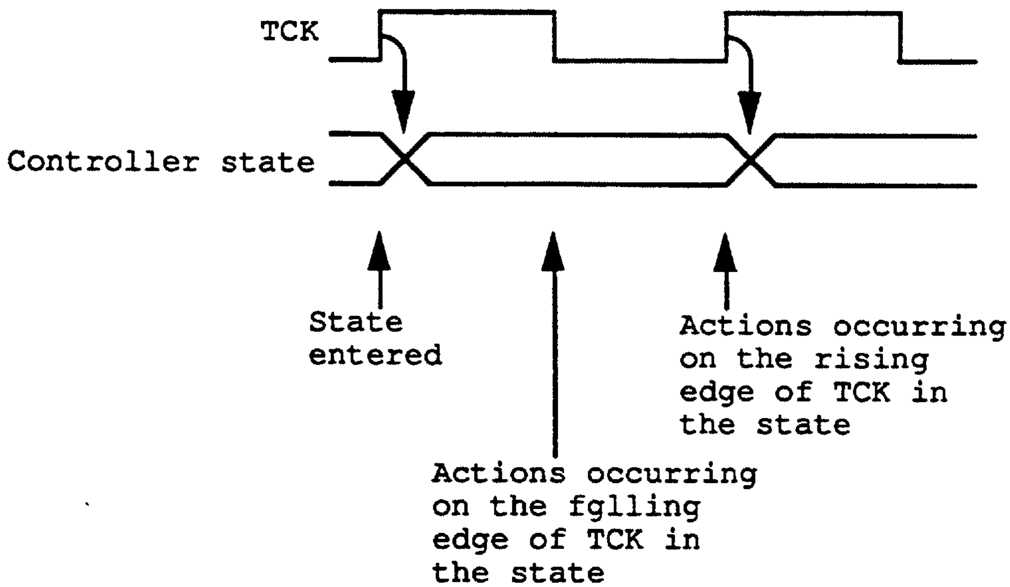


Fig 8.4-2 TAP Controller State Diagram

HEAD

Indicates the logical head number on the written data in media

SECTOR

Indicates the sector number

BYTES/SECTOR (MFM) / FORMAT BYTE (GCR)"

Code to indicate the data length in a sector (MFM).

Code to indicate the data length in a sector (GCR).

LAST SECTOR IN MULTI-SECTOR READ(or WRITE)

Indicates the last sector number to be accessed on the track

GAP3 (GAP3 Length)

Indicates the number of bytes to be written in GAP3

GSL (Gap3 Skip Length)

Indicates the number of bytes to be skipped in GAP3

DATA LENGTH IN BYTES

Specifies the data length per sector to be accessed only when the "Number of data bytes in the sector" is set to 0 in the FM format.

NCN (New Cylinder Number)

Indicates the cylinder number being seeked

PCN (Present Cylinder Number)

Indicates the cylinder number where the read/write head is located

ND (Non DMA transfer)

When this bit is 1(high), Non-DMA transfer mode is specified.

SYNC GROUPS(GCR)

Under Apple mode, specifies the number of the Self sync groups.

PARAMETERS USED IN THE MFM AND FM FORMATS

IAM is the special Address mark immediately after the Index position.

SYNC is the bytes that the PLL needs to synchronize with the input data from FDD before FDC read the ID field or the Data field.

IDAM is the special address mark in the ID field.

DAM is the special address mark in the Data field.

DDAM is the special address mark in the Data field, which is written by the Write Deleted Data.

CRC is the Check Redundancy Cyclic bytes.

Gap1 is located between the "IAM" and the SYNC bytes in the first sector immediately after the Index position.

Gap2 is located between the ID and Data fields.

Gap3 is located between Sectors.

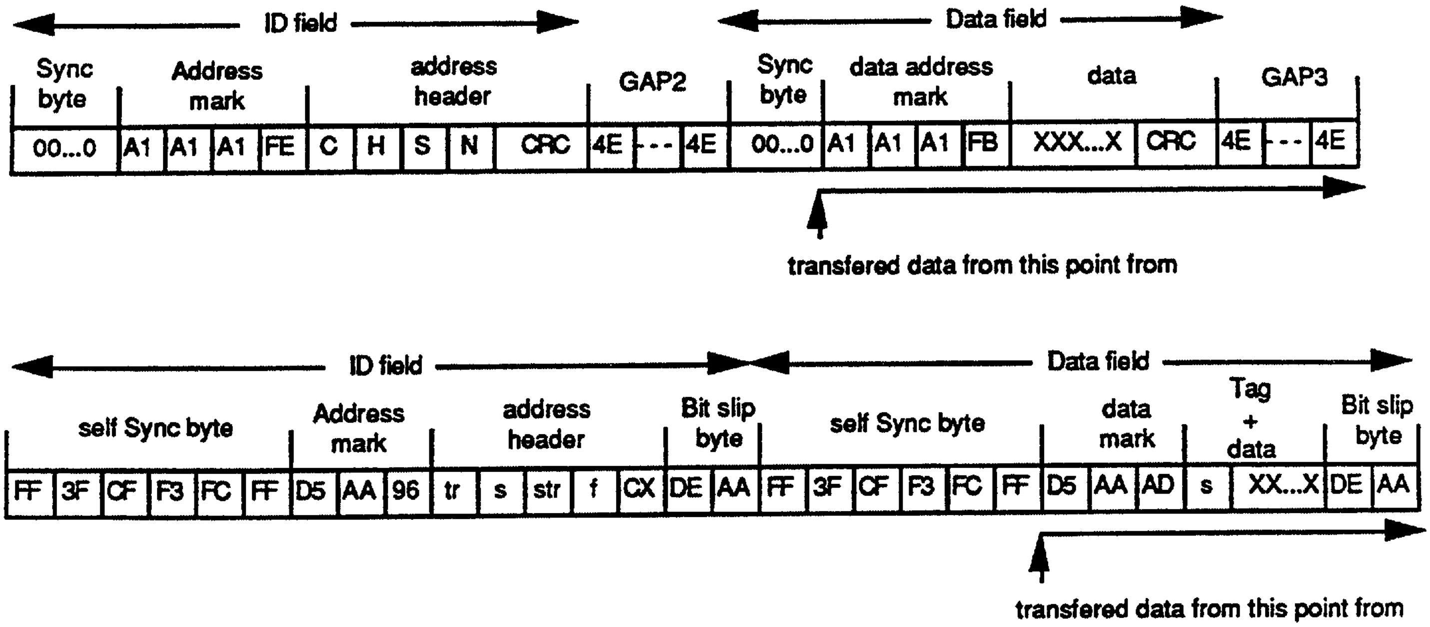


Fig. 4.18.2 Transferred Data for Dump After Specified ID Address Mark

Read A Track

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	FM	TB	0	0	0	1	0	command code
	W	X	X	X	X	X	HD	DR1	DR0	
	W	Cylinder								
	W	Head								
	W	Sector								
	W	(Bytes/Sector) / Format Byte								
	W	# of Sectors to be read								
	W	GSL(MFM) / don't care (GCR)								
	W	Data Length in Bytes								
Execution										data transfer between Host and FDD
	R	Status Regisiter 0								status information after this command
	R	Status Regisiter 1								
	R	Status Regisiter 2								
	R	Cylinder								
	R	Head								
	R	# of Sectors to be read								*1
	R	(Bytes/Sector) / Format Byte								

FUNCTION

Under Apple Mode:

This command is similar to the Read Data command, except that this is a continuous read operation where the data field in each of the sectors is read. Unlike multi-sector reads with the Read Data command, this command will read the sectors as they are encountered on the disk. However, by this command, FDC can only read the media with the sector number in physically sequential order (like 1, 2, 3, 4, ...). So, in the case of interleaved media (like 1, 9, 2, 10, ...), the FDC can not read the sectors sequentially, but will read the sectors as they encounter, which will set ND bit (also see the description of Status Register 1 on p. 42). Immediately after finding the sector specified in the command phase, the FDC starts reading all data fields on the track as continuous blocks of data. Even if the FDC finds an error in the Address header or Data Checksum bytes, it will continue to read the data from the track, but will mark the error in the Status register 0-2 in the result phase.

This command terminates when the number of sectors read is equal to the number specified in the command phase.

Seek

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Command	W	0	0	0	0	1	1	1	1	command code
	W	X	X	X	X	X	X	DR1	DR0	
	W	New CylinderNumber								
Execution										Head is positioned over specified cylinder.

FUNCTION

This command causes the FDD to retract the Read/Write head to the cylinder to be programmed in the "New cylinder Number" byte.

Under Apple mode:

The FDC executes this command by issuing the /Step command to the FDD. To determine that the /Step command has completed, the FDC reads the /Ready status line from the FDD. This provides a full handshake for the step operation. The following conditions are not supported by this command:

- Seek with no media installed
- Seek on more than one drive simultaneously
- Check status of the /DIRTIN signal during the seek operation

Under Standard modes:

The FDC operates this command if the internal parameter of "PCN" is not equivalent to the "New Cylinder Number"(NCN).

When NCN > PCN:

The DIR_B signal in the drive interface becomes active low and then the required number of the step pulses are issued to the FDD and the number of this PCN will be incremented per step pulse.

When NCN < PCN;

The DIR_B signal in the drive interface becomes inactive high and then the required number of the step pulses are issued to the FDD and finally the number of this PCN will be decremented per step pulse.

The interval time between the step pulses should set by the Step rate parameter in the Specify command. When PCN becomes equal to NCN, the SE bit in the Status register 0 is set and the FDC interrupts to

Select Drive Type

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
command	W	0	0	1	1	0	0	1	0	command code
command		X	X	X	X	X	X	D1	D0	Echo back for this command.

FUNCTION
The Select Drive Type command selects the type of drive that the next command will be executed on.

D1	D0	FDD
0	0	Conventional FDD (Reset Default) FDD =<4MB
0	1	13 MB FDD
1	0	RESERVED
1	1	APPLE FDD

The timing of SPECIFY command is shown in Fig.5.1-4. This command has only Command phase. The command codes, (SRT/HUT, and HLT under only Standard modes) and ND are written to the FDC in that order, and command execution terminates.

The timing of the SEEK and RECALIBRATE commands are shown in Fig.5.1-5. However, for the RECALIBRATE command the cylinder number to be sought is fixed (cylinder 0), and therefore the NCN parameter is not necessary. For either command, when the seeking operation to the desired location is confirmed, the FDC outputs the INT signal to the host to inform that seek operation is completed. In addition, these commands differ from other commands in that they have no Resultant phase. Consequently, result status are output in the R-phase of the SENSE INTERRUPT STATUS command given after the INT signal is confirmed.

The timing of the SENSE INTERRUPT STATUS command is shown in Fig.5.1-6. When the INT signal is output from the FDC and bit 4 (FDC Busy) of the status register is 0, this command checks the cause of the interrupt request. When this command is written, the FDC resets the RQM bit and INT signal and enters R-phase. The status at the time the interrupt is generated can be found by reading the contents of the ST0 and the PCN in the R- phase of this command.

The timing of the INVALID command is shown in Fig.5.1-10. The Invalid command is activated when either of the following occurs;

- If a command code not defined as a valid command is written in Command phase.
- If the SENSE INTERRUPT STATUS command is written but the cause of the interrupt no longer remains.

In either instance, 80(16) is set to the ST0 register to be read in Resultant phase as an invalid command and the FDC waits for the next command.

5.1.2 FIFO Operations

The FDC has the FIFO and all the data transfer can go through the FIFO. The FIFO is 16 bytes in size and programmable threshold value. In this description, "threshold" is defined as the number of available bytes to the FDC until the HOST starts the service from the FDC request, and range from 1 to 16. The threshold parameter which the user programs is one less and range from 0 to 15. The FDC can support the single and demand transfer. After a reset, the FIFO is no available. This reset default is changed by issued "CONFIGURE" command, and the FIFO operation becomes available with threshold control. The effectivity of FIFO is that it can allow the system a larger DMA latency without causing a overrun/underrun error.

In command phase, the command and their parameters must be sent by checking RQM=1 and DIO=1 of status register. After receives all

MAX SERVICE DELAY

The service latency is defined by the following formula:

Delay = Threshold x (8bits/data rate)-12 x internal clock period

for example from HOST to FDC   Threshold = 8 bytes Data Rate=0.5Mbps

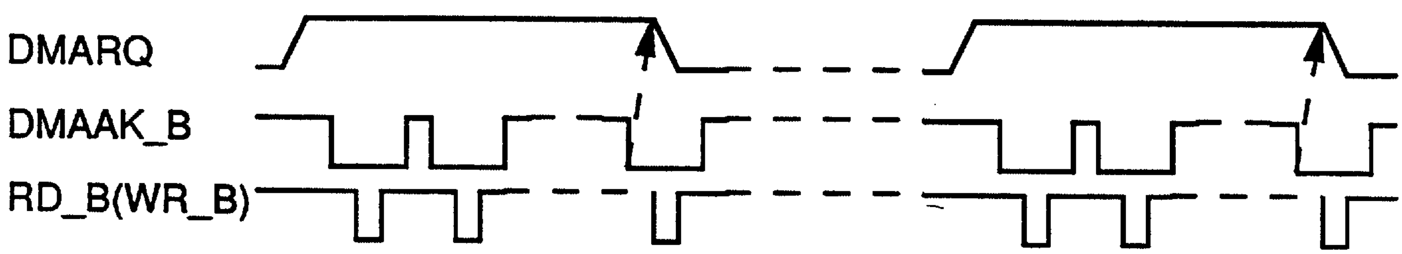
8byte x (8bits/0.5μsec) -12x0.125usec = 126.6uSec

5.1.2.2 DMA Modes

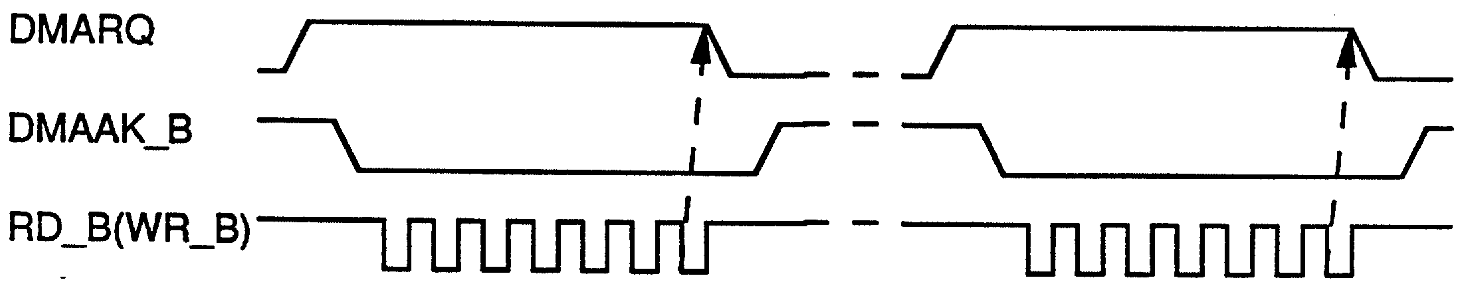
There are two DMA Data Transfer modes:

(1) Single Transfer mode

(2) Demand Transfer mode



Single Transfer Mode



Demand Transfer Mode

Fig. 5.1.2.1 Host Interface During the DMA transfers

Data Transfers from FDC to HOST

When the number of bytes in FIFO is less than or equal to <16 - threshold>, a DMARQ is activated. By the FDC request, a DMA controller starts data transfer from FIFO to HOST. The FDC will deactivate the DMARQ when FIFO becomes empty. DMARQ goes inactive after DMAAK goes active for the last byte of a data transfer (in DMA controller's single transfer mode) or on

the active edge of RD_B on the last byte(in DMA controller's demand transfer mode).

DataTransfers from HOST to FDC

When then number of bytes in FIFO is greater than of equal to <threshold>, a DMARQ is actives. By the FDC request, a DMA controller starts data transfer from HOST to FIFO. The FDC will deactivate the DMARQ when FIFO become full. DMARQ goes inactive after DMAAK goes active for the last byte of a data transfer (in DMA controller's single transfer mode) or on the active edge of WR_B the last byte(in DMA controller's demand transfer mode).

5.1.3 Non-DMA mode

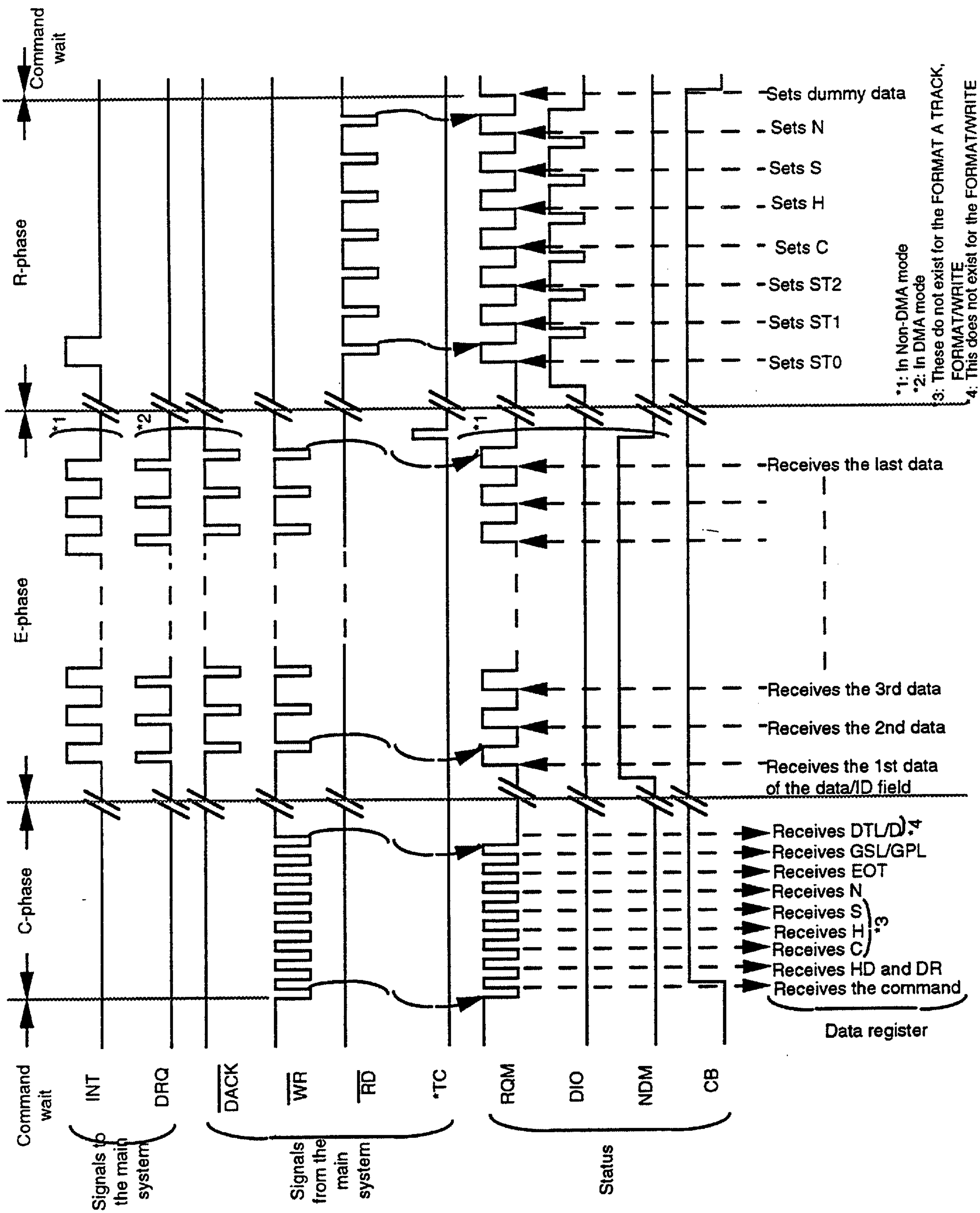
Data Transfers from FDC to HOST

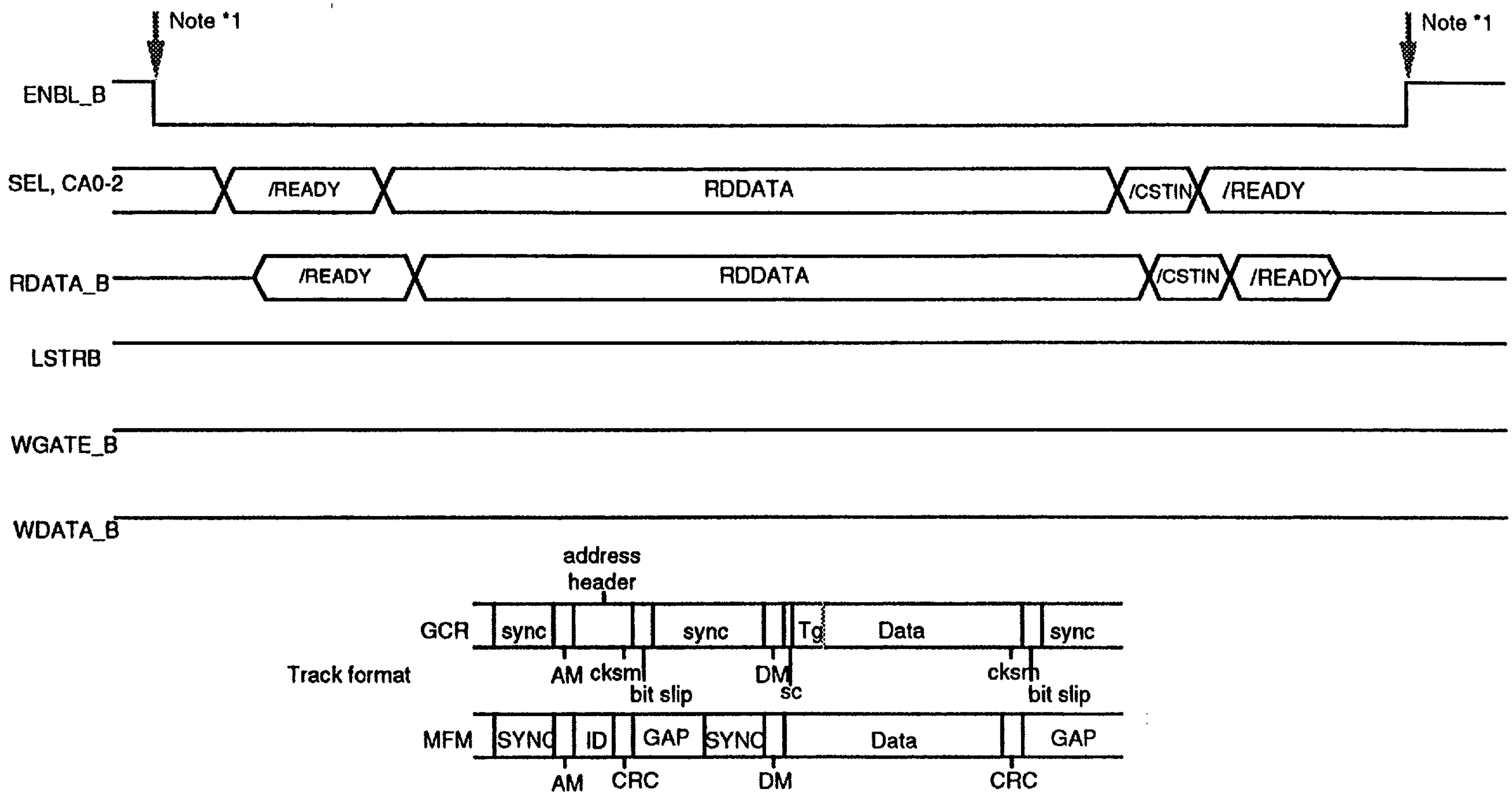
The INT and RQM bit in the Main Status Register are activated when the number of bytes in FIFO is less than or equal to the <16-threshold>. The HOST must start to read the data from the FIFO by request the FDC, and repeat until the data in the FIFO is empty. The FDC will deactivate the INT and RQM bit when the FIFO becomes empty.

Data Transfers from HOST to FDC

The INT and RQM bit in the Main Status Register are activated when the number of bytes in FIFO is greater than or equal to the <threshold>. The HOST must start to write the data to the FIFO by request the FDC, and repeat until the data in FIFO are full. The FDC will deactivate the INT and the RQM bit when the FIFO becomes full.

Fig.5.1-2 WRITE DATA, FORMAT A TRACK, and FORMAT/WRITE commands

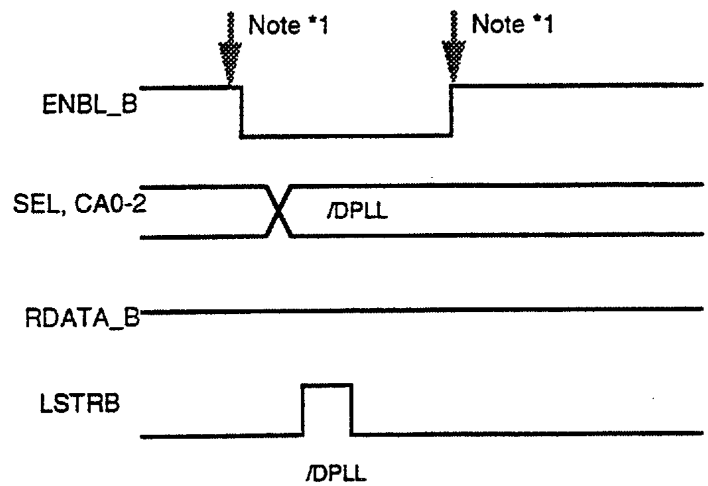




Note *1 : This signal can be controlled by the only "Set Enable Control" command.

Fig.5.2-1 READ DATA, READ ID, READ A TRACK, and RAW DUMP

Fig.5.2-7 Disable/Enable DPLL



Note *1 : This signal can be controlled by the only "Set Enable Control" command.

Fig.5.2-8 SET DRIVE MODE

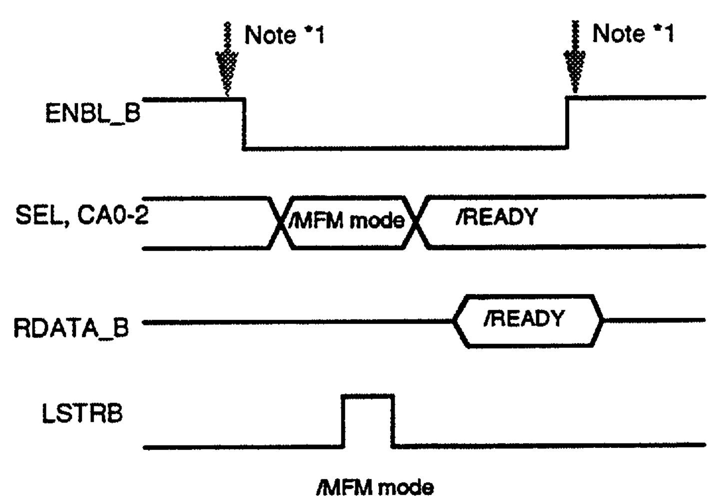
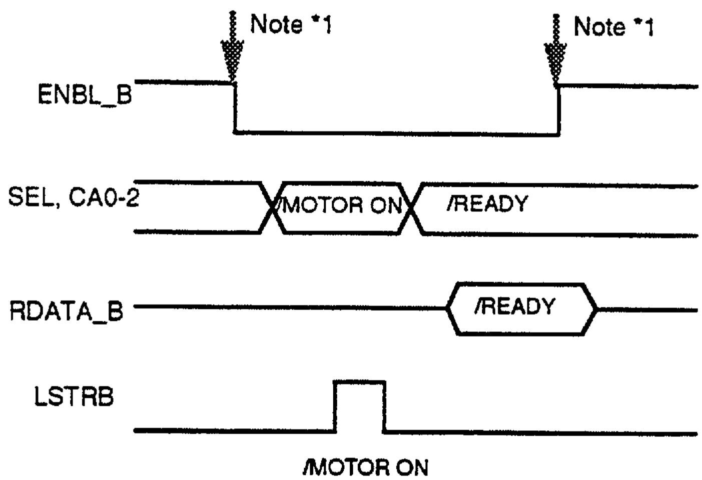
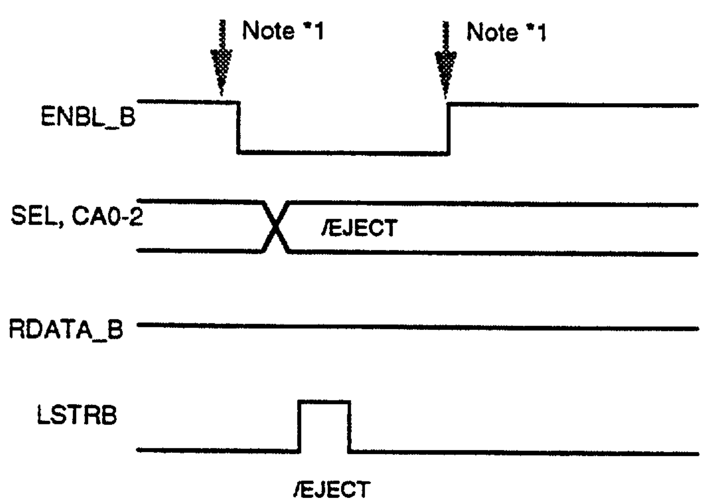


Fig.5.2-9 SET MOTOR CONTROL for Motor ON



Note *1 : This signal can be controlled by the only "Set Enable Control" command.

Fig.5.2-10 EJECT

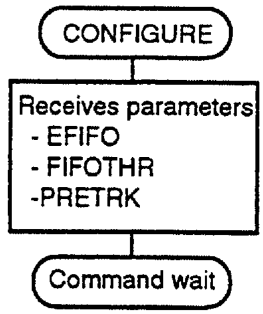


Chapter 6 Firmware Flowcharts

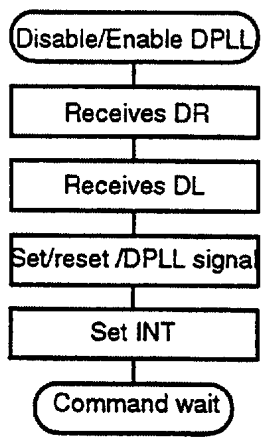
Under Apple mode, abstract firmware algorithms for each command are shown at the following pages.

Under Standard modes, the abstract firmware algorithms are the same as that of the µPD765A.

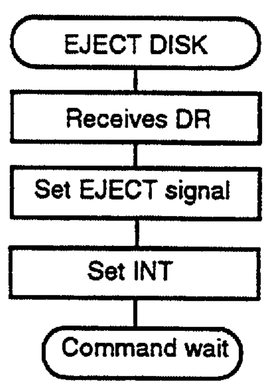
CONFIGURE



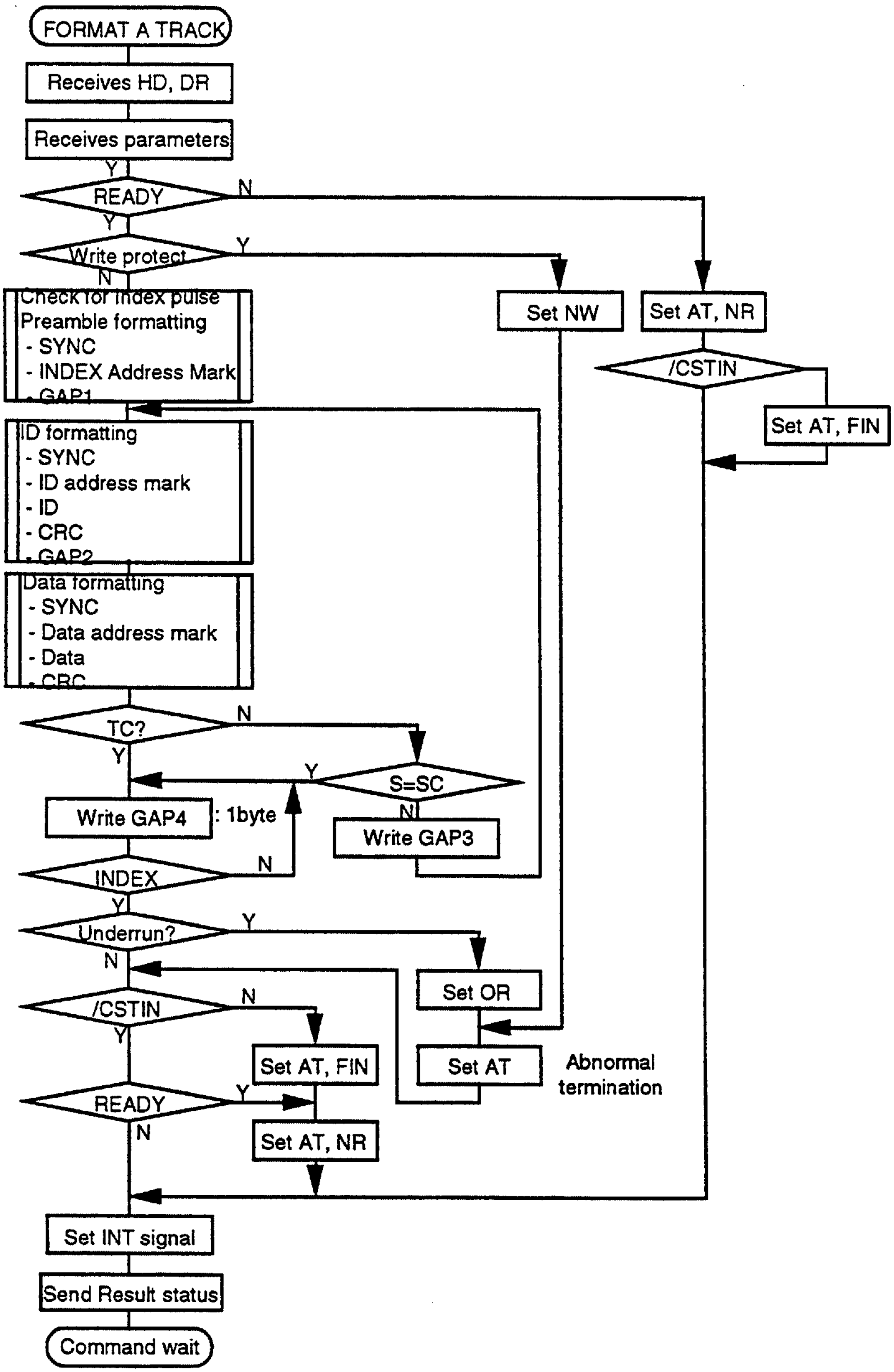
DISABLE/ENABLE DPLL



EJECT DISK



FORMAT A TRACK (MFM Format)



READ ID (GCR Format)

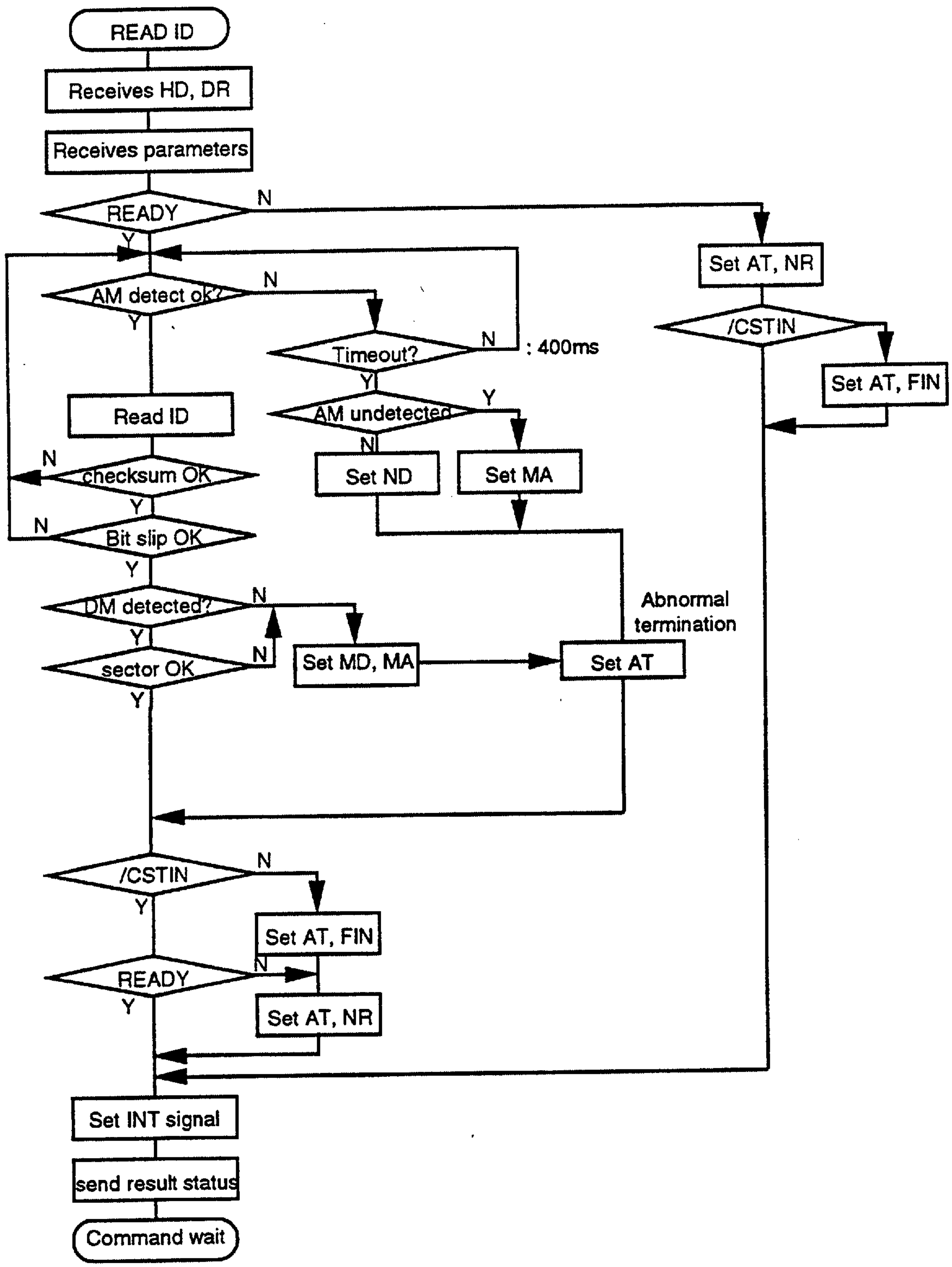


Fig.8 MFM FDD Control Timing

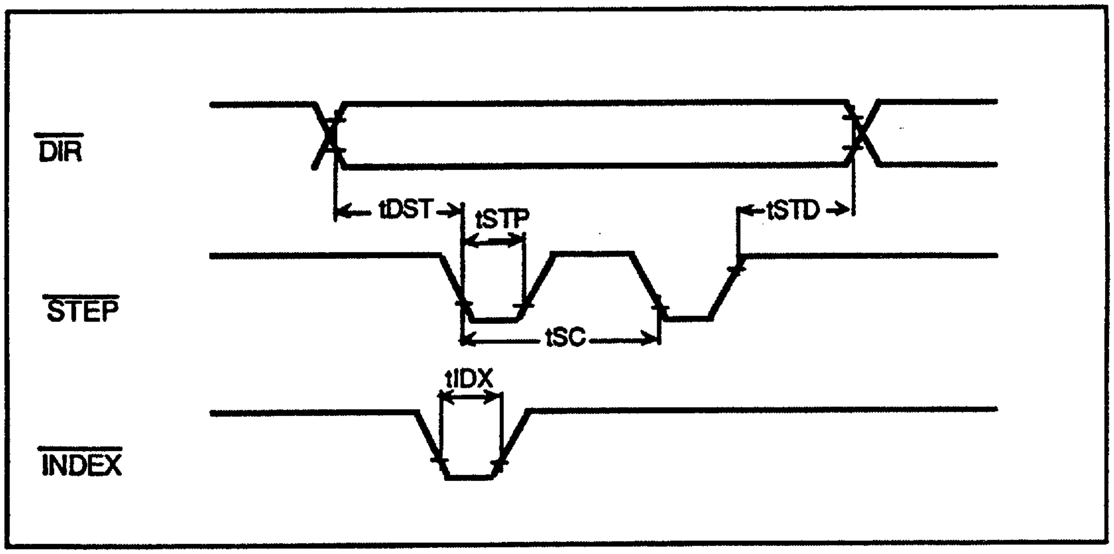


Fig. 9 Negative Reset